CM-120 USB 7-in-1 Combo Card Reader Controller Datasheet

Version 1.3

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1.DESCRIPTION AND OVERVIEW

Overview
CM120 is a USB 1.1 full speed 7-in-1 controller for Combo Card Reader, applicable for major MB / NB chipsets of Intel, VIA, Ali, and SIS. CM120 is suitable for PC2001-compliant desktops, notebook computers, and any other platforms with USB host controller port.

Plug and Play
CM120 provides friendly plug and play function, and by using the select pin the power can be switched between usb bus power (500mA) or self power (100mA). It only takes one 12MHz crystal input to provide provides internal 48MHz PLL frequency for USB system operation. It is a popular purpose USB interface reader/writer controllers which integrates PLL, embedded data buffer and high performance engine. It comprises SPI (HID) mode to external MCU and 16 bits GPIO for user-friendliness.

7-in-1 Card Interface
CM120 comprises six mainstream card interfaces: Compact Flash Card (CF) / Microdrive, Smart Media Card (SM) / eXtreme Digital Card (xD) , Multi Media Card (MMC) / Secure Digital Card (SD) and Memory Stick Card (MS).

Cost-effectiveness
As to the cost concern, CM120 integrates the processor and embedded data buffer. In that regard, it does not need any external memory module or others bom materials .

Features

- USB 1.1 Full Speed
- Compliant with USB Storage device class specifications
- Compliant with USB HID device specification v1.0
- Fixed USB full speed mode 12Mbits/s
- Uses 3 sets Endpoint control, two bulk pipes, and one control pipe
- USB bus power and self power capability. Low power consumption
- Internal PLL, need only 12MHz crystal to provide 48MHz frequency
- Fully Support Compact Flash (CF) card / Microdrive card interface
- Fully Support Smart Media (SM) / eXtreme Digital (xD) card interface
- Fully Support Multi Media card (MMC) / Secure Digital card (SD) interface
- Fully Support Memory Stick card (MS) interface
- Capable of preventing inappropriate card plug-out via the utilization of time out mechanism
- Support SPI mode interface
- Support 5 kinds of LED display for USB/CF/SD/SM/MS to indicate operation status
- Support 16 bits general purpose input and output
- Available 100 QFP package.

PIN DESCRIPTIONS

CM 120

Pin No.	Pin Name	Pin Type	Description
1	VDD1	P	Digital POWER 3.3V
2	XTEST	I_S/P_L	Testmode enable
3	XMS_DATA	B/P_H	Memory Stick data bus
4	XMS_CLK	O	Memory Stick clock output
5	XMS_BS	O	Memory Stick bus state output
6	XMS_DETN	I_S/P_H	Memory Stick card detect low active
7	VSS1	P	Digital GND
8	AVSS	P	PLL Analog GND
9	XTAL1	I/A	12MHz Crystal Input
10	XTAL2	O/A	12MHz Crystal Output
11	AVDD	P	PLL Analog power 3.3V
12	XSMXD_DETN	I_S/P_H	SmartMedia / xD card detect low active
13	XSMXD_RBN	I/P_H	SmartMedia / xD ready busy low active
14	XSM_WPSWN	I_S/P_H	SmartMedia write protect low active
15	XSMXD_ALE	O	SmartMedia / xD address latch enable
16	XSMXD_CLE	O	SmartMedia / xD command latch enable
17	VDD2	P	Digital POWER 3.3V
18-25	**XSMXD_DATA [7:0]**	B/P_L	**SmartMedia / xD data bus [7:0]**
26	XSMXD_REN	O	SmartMedia / xD read command
27	XSMXD_WEN	O	SmartMedia / xD write command
28	VSS2	P	Digital GND
29	VSS3	P	Digital GND
30	XSMXD_CEN	O	SmartMedia / xD chip enable
31	XSMXD_WPN	O	SmartMedia / xD write protect output
32	XSP_CLK	I_S	SPI mode clock output
33	XSP_DI	I	SPI mode data input
34	XSP_DO	O	SPI mode data output
35	XSP_CS	I	SPI mode chip select output
36	XSELFPWR	I_S/P_L	USB self power enable
37	XPDN	O	Power Save for external Device low active
38	XENHID	I_S/P_L	HID enable
39	XRSTN	I_S/P_H	System reset input low active
40	VDD3	P	Digital POWER 3.3V
41-48	**XGPIO[0:7]**	B/P_L	**GPIO data bus [0:7]**
49	XMS_PWR_EN/XGPIO[8]	B/P_L	Memory Stick power enable low active

Pin No.	Pin Name	Pin Type	Description
50-52	**XCF_SA[0:2]**	O	**CF/Microdrive address bus [0:2]**
53	VSS7	P	Digital GND
54	VDD4	P	Digital POWER 3.3V
55	XCF_IORN	O	CF/Microdrive I/O read low active
56	XCF_IOWN	O	CF/Microdrive I/O write low active
57-58	**XCF_CS[0:1]N**	O	**CF/Microdrive chip select bus [0:1]**
59	XCF_DETN	I/P_H	CF/Microdrive card detect low active
60	VSS4	P	Digital GND
61-68	**XCF_DATA[0:7]**	B/P_L	**CF/Microdrive data bus [0:7]**
69	VDD5	P	Digital POWER 3.3V
70-77	**XCF_DATA[8:15]**	B/P_L	**CF/Microdrive data bus [8:15]**
78	XCF_ORSTN	O	CF/Microdrive resest output low active
79	XCF_PWR_EN	O	CF/Microdrive power output enable
80	VSS5	P	Digital GND
81	VSS6	P	Digital GND
82	XSD_WPN	I_S/P_H	SD/MMC write protect high active
83	XSD_DETN	I_S/P_H	SD/MMC card detect low active
84	XSD_CLK	O	SD/MMC clock output
85	XSD_CMD	B/P_H	SD/MMC command/response
86-89	**XSD_DATA[0:3]**	B/P_H	**SD/MMC data bus[0:3]**
90	VDD6	P	Digital POWER 3.3V
91	XSMXD_PWR_EN /XGPIO[9]	B/P_L	SmartMedia / xD power enable low active
92	XSD_PWR_EN / XGPIO[10]	B/P_L	Secure Digital power enable low active
93	XCF_LED / XGPIO[11]	B/P_L	CF/Microdrive access LED display
94	XSD_LED / XGPIO[12]	B/P_L	SD/MMC access LED display
95	XSMXD_LED / XGPIO[13]	B/P_L	SmartMedia / xD access LED display
96	XMS_LED / XGPIO[14]	B/P_L	MemoryStick access LED display
97	XUSB_LED / XGPIO[15]	B/P_L	USB access LED display
98	XUSBGND	P	USB Analog GND
99	XDP	A/B	USB data plus
100	XDM	A/B	USB data minus

Note 1. I : Input pin ; O : Output pin ; B : Bi-direction pin
2. I_S : Schmitt trigger input

3. P_L : Internal pull low
4. P_H : Internal pull high
5. A : Analog PAD

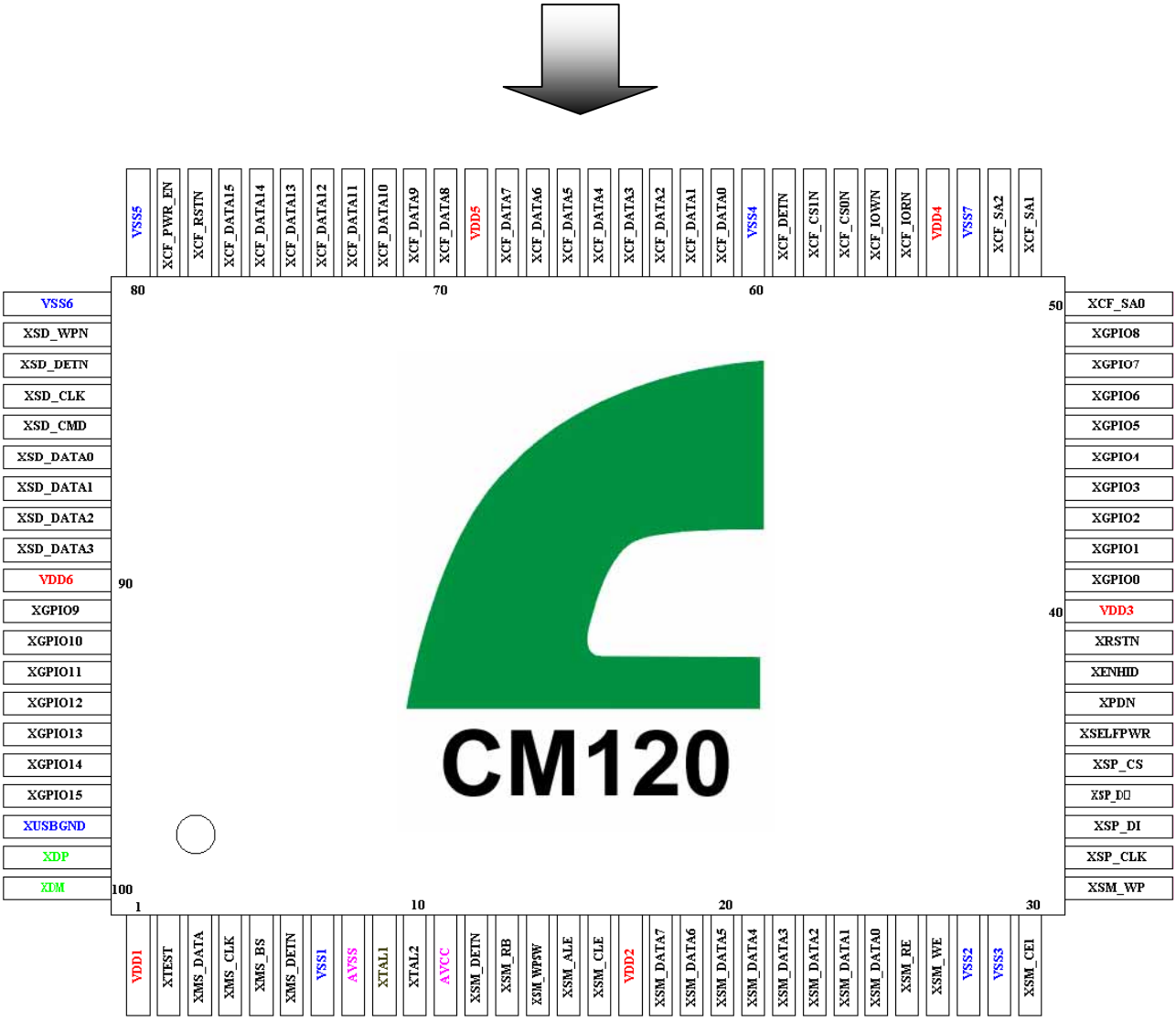


Figure 1. Pin Assignments (Top View)

CM120 7-in-1 USB combo card reader is designed according to the Universal Serial BUS(USB) Mass Storage Class specifications, capable of managing the file access and file format, dead lock avoidance, card detection, write protection, ECC corecation and detection, custiomized icon name and LED display in PC environment. It includes:

- **File Management:** file read/write, file delete, file copy, file execution and format.
- **Dead Locking Avoidance**：prevent users from inappropriate card plug-out card or other some unreasonable access via the utilization of time out mechanism.
- **Card Detection**：CF/Microvdrive, SD/MMC, SM/xD, MS card detection.
- **ECC Corecation & Detectoion**：SmartMedia (SM) / eXtreme Digital (xD) and Memory Stick (MS) support one bit ECC correcation and two bits ECC detection.
- **Custiomized Icon Name**：Provide customized name and iocn for each disk in file manager.
- **LED Display**：Provide 5 kinds LED dipslay with 1) USB access, 2) CF/Microdrive access, 3) SD/MMC access, 4) SM/xD access and 5) MS access. Sink current is 8mA.
- **SPI Mode**：Support SPI mode to process external MCU to access HID function.
- **16 bits GPIO**：Support 16 bits general purpose input nand output for user-friendliness.

SOURCE	PIN NAME	PIN Position
CF/Microdrive	XCF_SA[0:2], XCF_IORN, XCF_IOWN, XCF_CS[0:1]N, XCF_DETN, XCF_DATA[0:15], XCF_RSTN, XCF_PWR_EN	50~52,55,56,57~58,59,61~68,70~77,78,79
SD/MMC	XSD_WPN, XSD_DETN, XSD_CLK, XSD_CMD, XSD_DATA[0:3], XSD_PWR_EN	82,83,84,85,86~89
SM/xD	XSMXD_DETN, XSMXD_RB, XSM_WPSW, XSMXD_ALE, XSMXD_CLE, XSMXD_DATA[7:0], XSMXD_RE, XSMXD_WE, XSMXD_CE1, XSMXD_WP, XSMXD_PWR_EN	12,13,14,1516,18~25,26, 27,30,31,91
MS	XMS_DATA, XMS_CLK, XMS_BS, XMS_DETN, XMS_PWR_EN	3,4,5,6,49
SPI	XSP_CLK, XSP_DI, XSP_DO, XSP_CS	32,33,34,35
LED	XUSB_LED, XMS_LED, XSM_LED, XSD_LED, XCF_LED	97,96,95,94,93
GPIO	XUSB_LED, XMS_LED, XSMXD_LED, XSD_LED, XCF_LED, XSD_PWR_EN, XSMXD_PWR_EN, XMS_PWR_EN, XGPIO[7:0]	97~91,49~41
Misc	XTEST, XSELFPWR, XPDN, XENHID, XRSTN, XDP, XDM	2,36,37,38,39,99,100
POWER	VDD1,AVCC,VDD2,VDD3,VDD4,VDD5,VDD6	1,11,17,40,54,69,90
GND	VSS1, AVSS, VSS2, AVSS3, AVSS7, AVSS4, AVSS5, AVSS6, XUSBGND	7,8,28,29,53,60,80,81,98

*Note: DI – digital input pin , DO – digital output pin, DIO – digital bi-directional pin, P – power pin, PD – pull down with 100K Ohm resistor, AI – analog input, AO – analog output

Block diagram of CM120

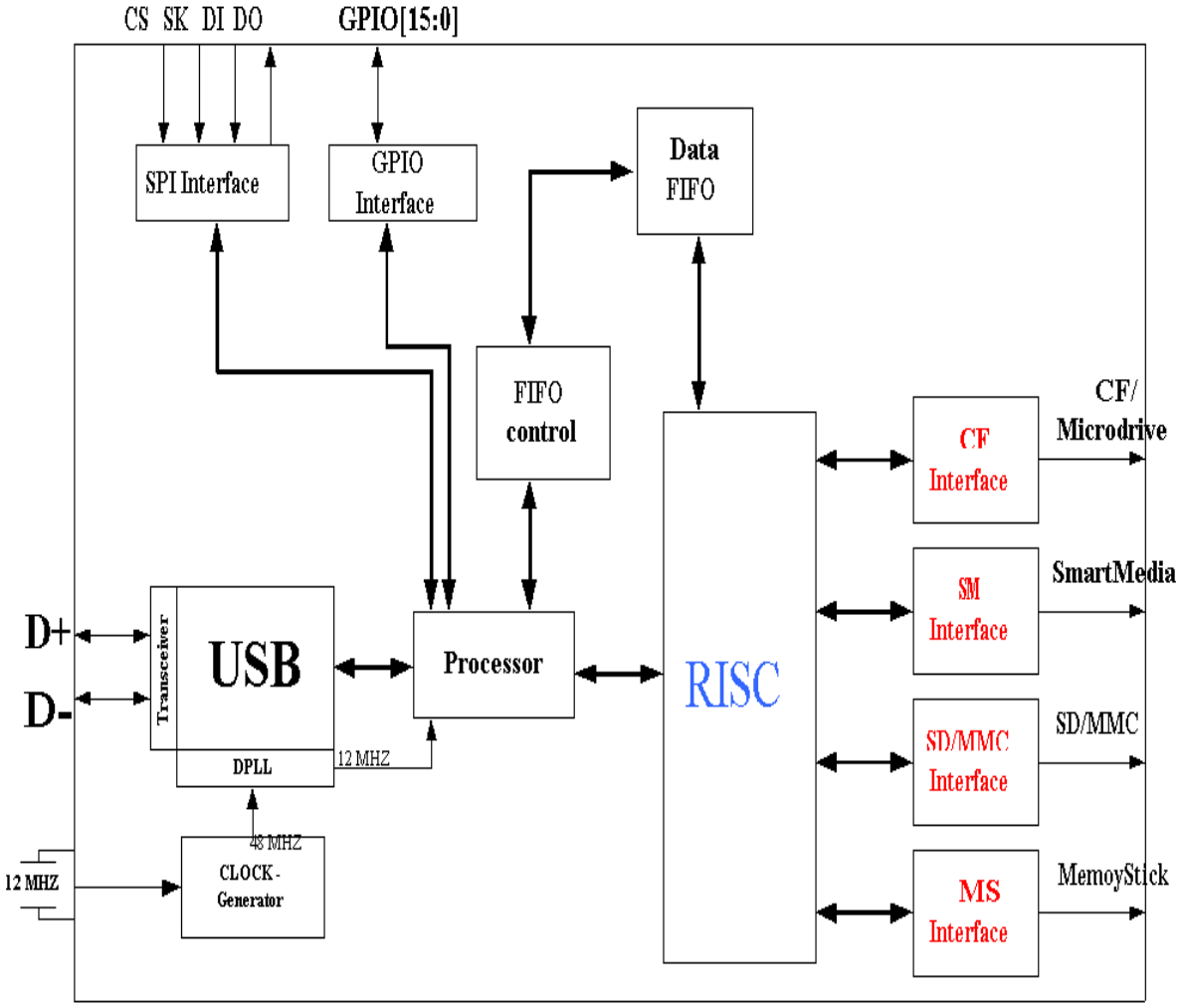


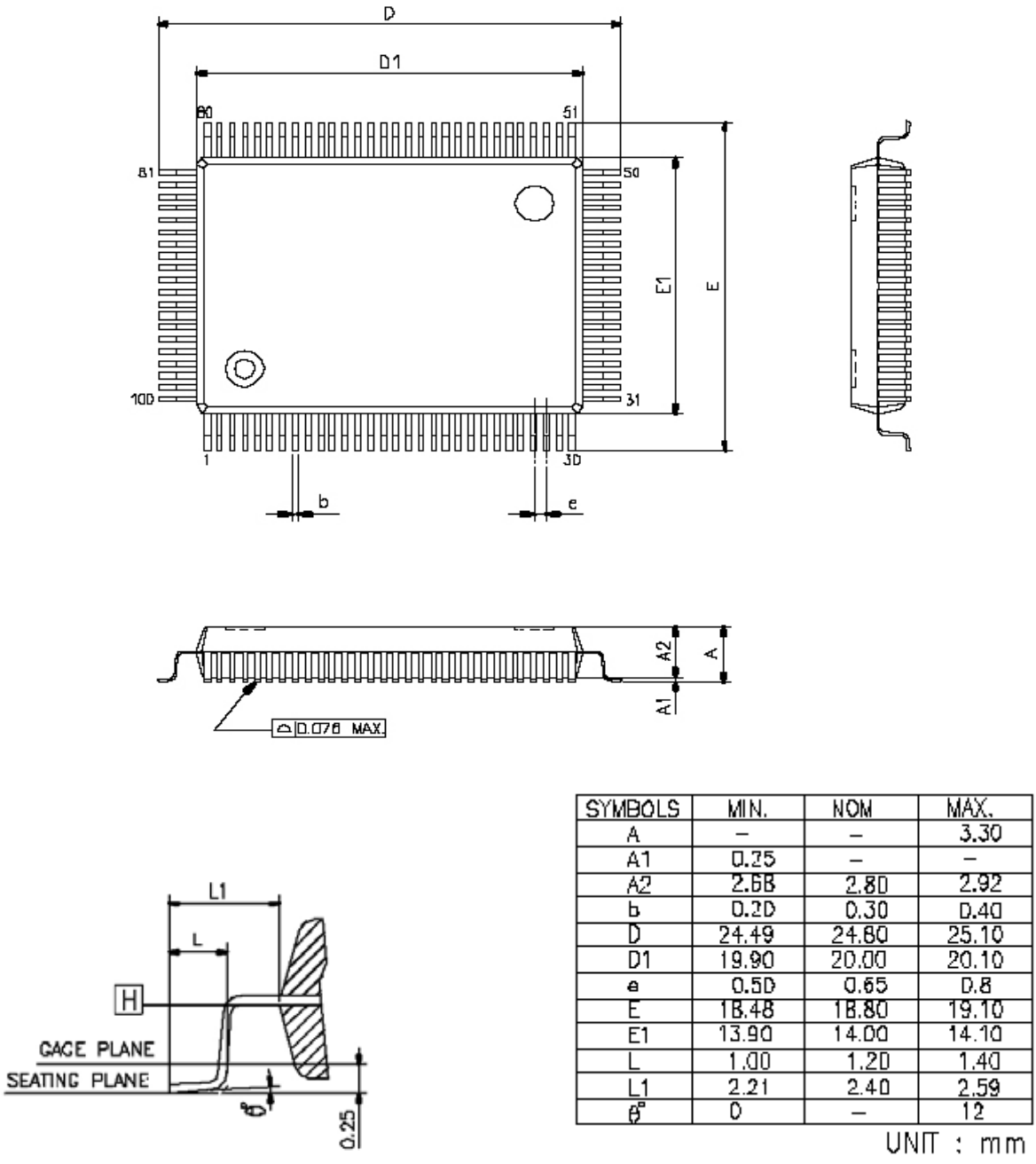
Figure 2：Block Diagram Of CM120

2. ORDERING INFORMATION

Model Number	Package	Operating Ambient Temperature	Supply Range
CM120	100-Pin QFP	0^{o} C to $+70^{o}$ C	DVdd =3.3V, AVdd = 3.3V

Outline of Dimensions Dimensions shown in inches and (mm)

◆100 Pin QFP

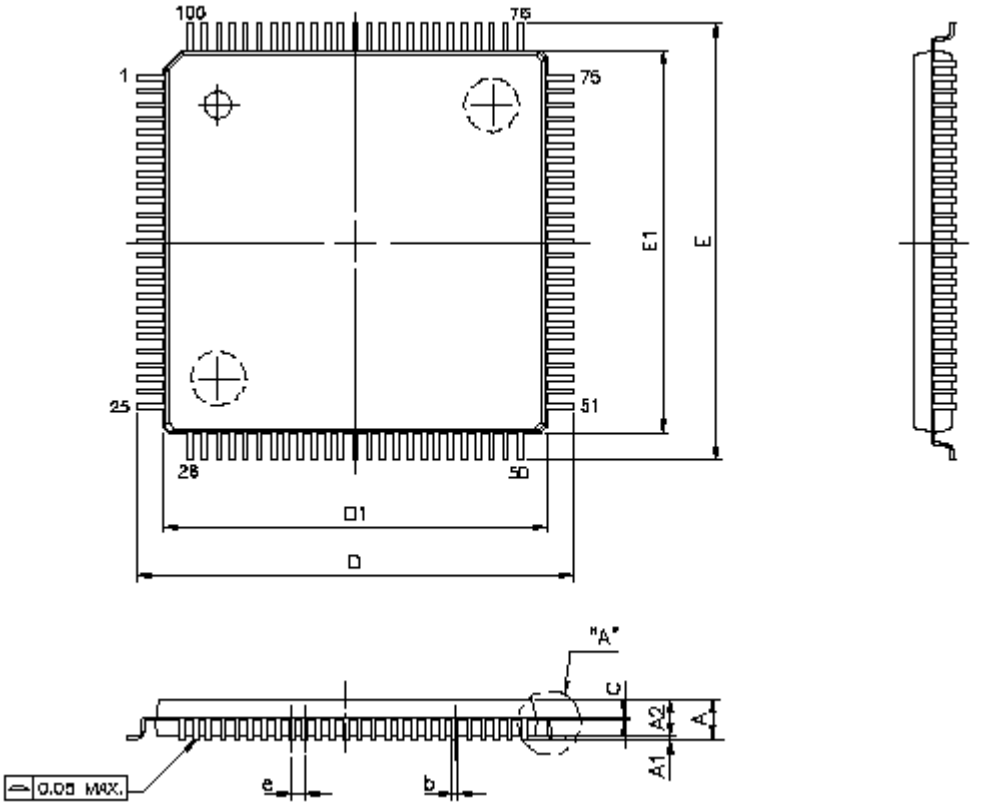


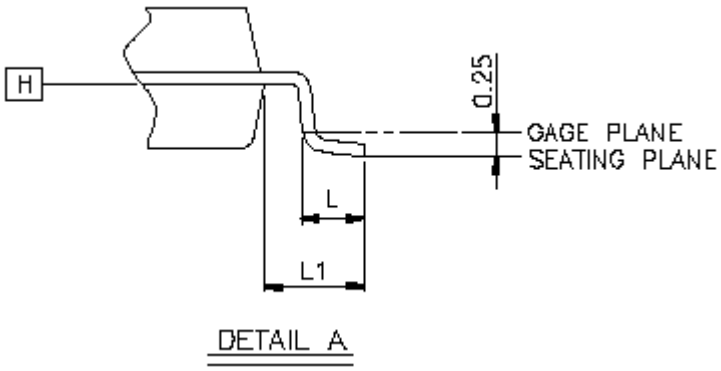
SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.30
A1	0.25	–	–
A2	2.68	2.80	2.92
b	0.20	0.30	0.40
D	24.49	24.80	25.10
D1	19.90	20.00	20.10
e	0.50	0.65	0.8
E	18.48	18.80	19.10
E1	13.90	14.00	14.10
L	1.00	1.20	1.40
L1	2.21	2.40	2.59
θ°	0	–	12

UNIT : mm

Figure 3：Mechanical Dimension of CM120

◆100 Pin LQFP





VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Figure 3.1：Mechanical Dimension of CM120L

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3. PIN / SIGNAL DESCRIPTIONS

3.1 USB & Misc I/O SIGNALS

These signals connect CM120 to USB host controller counterpart, external crystal, multi-power selection, general purpose control and external MCU component.

Table 1：USB & Misc Signal List

Signal Name	Type	Description
XDP	I/O	USB data plus signal
XDN	I/O	USB data minus signal
XTEST	I	Testmode enable
XTAL1	I	12 MHz crystal input
XTAL2	O	12 MHz crystal output
XSELFPWR	I	USB self power enable
XPDN	O	USB power down enable
XENHID	I	HID function enable
XRSTN	I	System reset input
XSP_CLK	I	SPI mode clock input
XSP_DI	I	SPI mode data input
XSP_DO	O	SPI mode data output
XSP_CS	I	SPI mode chipselect input
XGPIO[7:0]	I/O	General purpose input and output

3.2 CF & Microdrive I/O SIGNALS

These signals connect CM120 to analog sources and sinks, including microphones and speakers.

Table 2：CF/Microdrive Signal List

Signal Name	Type	Description
XCF_SA[2:0]	O	CF/Microdrive addressbus[2:0] output
XCF_IORN	O	CF/Microdrive read command output
XCF_IOWN	O	CF/Microdrive write command output
XCF_CS[1:0]N	O	CF/Microdrive chip select bus output
XCF_DETN	I	CF/Microdrive card detect input
XCF_DATA[15:0]	I/O	CF/Microdrive data bus
XCF_RSTN	O	CF/Microdrive reset output
XCF_PWR_EN	O	CF/Microdrive power enable output
XCF_LED	O	CF/Microdrive LED output

3.3 SD/MMC I/O SIGNALS

Table 3：SD/MMC Signal List

Signal Name	Type	Description
XSD_WPN	I	SD/MMC write protect input
XSD_DETN	I	SD/MMC card detect input
XSD_CLK	O	SD/MMC clock output
XSD_CMD	I/O	SD/MMC command response
XSD_DATA[3:0]	I/O	SD/MMC data bus
XSD_PWR_EN	O	SD/MMC power enable output
XSD_LED	O	SD/MMC LED output

3.4 SM / xD I/O SIGNALS

Table 4：SM Signal List

Signal Name	Type	Description
XSMXD_DETEN	I	SM / xD card detect input
XSMXD_RB	I	SM / xD read/busy input
XSM_WPSW	I	SM write protect input
XSMXD_ALE	O	SM / xD address latch output
XSMXD_CLE	O	SM / xD command latch output
XSMXD_DATA[7:0]	I/O	SM / xD data bus
XSMXD_RE	O	SM / xD read command output
XSMXD_WE	O	SM / xD write command output
XSMXD_CE1	O	SM / xD chip enable output
XSMXD_WP	O	SM / xD write protect output
XSMXD_PWR_EN	O	SM / xD power enable output
XSMXD_LED	O	SM / xD LED output

3.5 MS I/O SIGNALS

Table 5：MS Signal List

Signal Name	Type	Description
XMS_DATA	I/O	MS data bus
XMS_CLK	O	MS clock output
XMS_BS	O	MS bus state output
XMS_DETN	I	MS card detect input
XMS_PWR_EN	O	MS power enable output
XMS_LED	O	MS LED output

3.6 POWER AND GROUND SIGNALS

Table 6：Power and Ground Signal of CM120

Signal Name	Type	Description
VDD1	P	Digital power Vdd = 3.3V
VDD2	P	Digital power Vdd = 3.3V
VDD3	P	Digital power Vdd = 3.3V
VDD4	P	Digital power Vdd = 3.3V
VDD5	P	Digital power Vdd = 3.3V
VDD6	P	Digital power Vdd = 3.3V
VSS1	P	Digital ground
VSS2	P	Digital ground
VSS3	P	Digital ground
VSS4	P	Digital ground
VSS5	P	Digital ground
VSS6	P	Digital ground
VSS7	P	Digital ground
XUSBGND	P	Analog ground
AVCC	P	Analog power Vdd = 3.3V
AVSS	P	Analog ground

4. SYSTEM INTERFACE

4.1 System

All USB device command/status information intertransmit data over USB bus with four signals (D+, D-, VBUS, GND) cable. The system interface of the signals connecting the CM120 is shown in Figure 1. It includes clock generator, reset, processor, risc, fifo control, data memory, CF/Microdrive interface, SmartMedia interface, SD/MMC interface, Memory Stick interface, SPI and GPIO.

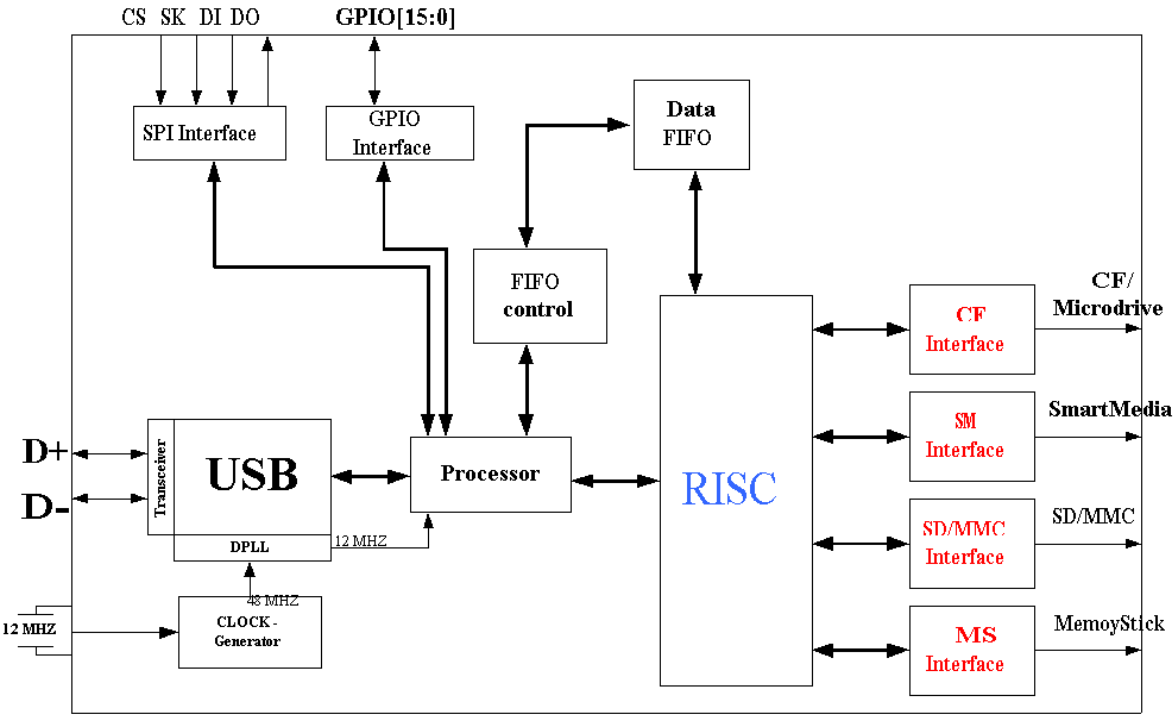


Figure 4. CM120 block diagram

4.2 CLOCK Generator

CM120 generates its clock internally from an externally connected 12MHz crystal clock source through the XTAL1 pin. Internal PLL function provides 48MHz for USB operation.

The beginning of all USB packets or frames transmitted over USB bus needs one 4X12 MHz to decode the correct phase information. Subsequently, it is sampled on the receiver side of CM120 on each immediately followed rising edge of PLL 48MHz clock.

4.3 RESETTING

There are 3 types of reset detailed under “Timing Characteristics”：

1. A Power-on reset where all CM120 logic (registers included) is initialized to its default state
2. A System reset where the contents of the CM120 register set are left unaltered
3. A Register reset which only initializes the CM120 registers to their default states

4.4 CF/Microdrive INTERFACE PROTOCOL

The CompactFlash interface contains a 50-pin connector to CompactFlash Storage Card or Microdrive. The CF interface of the chip can be connected to either type I CF or type II Microdrive flash card.

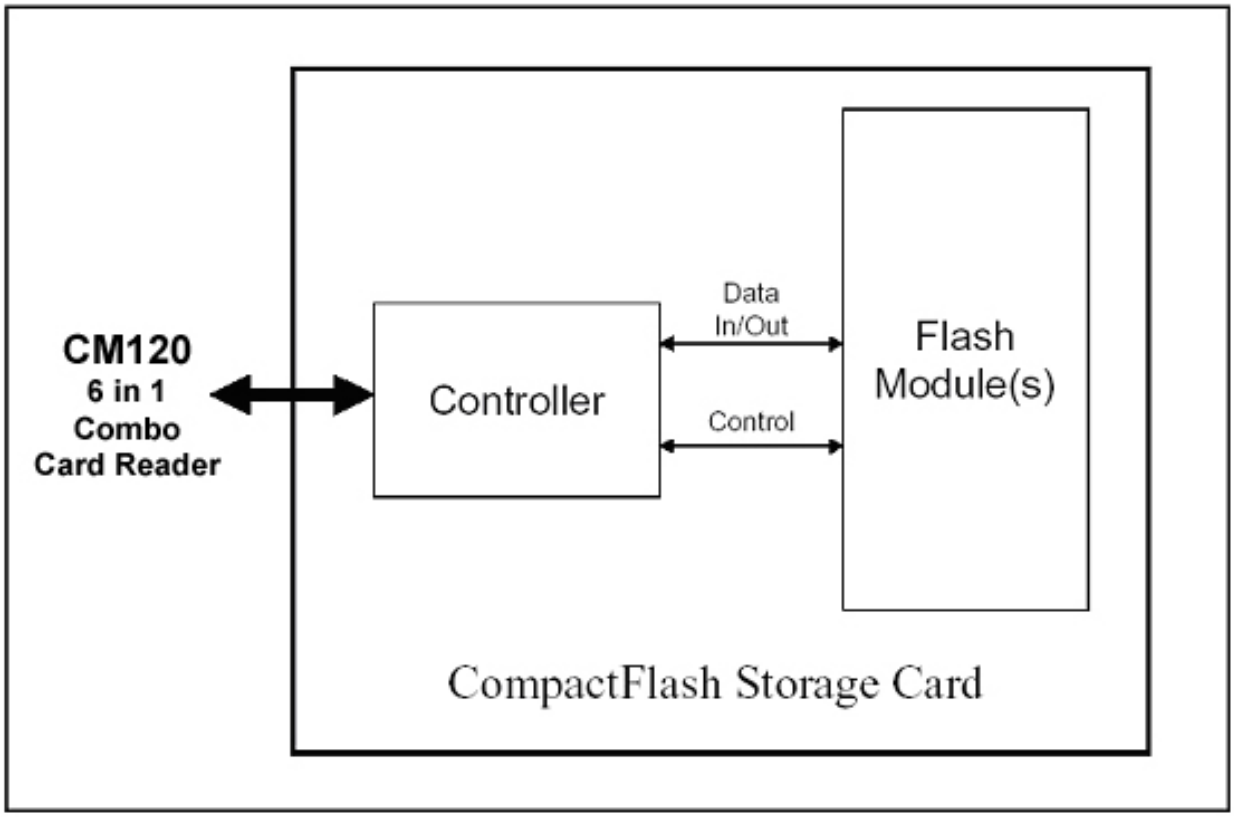


Figure 5:CpmpactFlash Storage Card Block Diagram

The Figure 25 and Figure 26 are the I/O read/write waveform for our CF bus protocol in True IDE Mode. The I/O read/write timing can be referenced on CF+ & CF SPECIFICATION REV. 1.4 . The I/O decoding method is listed in table 7. It is obvious that the figure 8 is the read status cycle, and the figure 9 is the write data cycle.

Table 7：CF True IDE Mode I/O Decoding

XCF-S1N	XCF-CS0N	XCF_SA2	XCF_SA1	XCF_SAD	XCF_IORN=0	CXF_IOWN=0
1	0	0	0	0	RD DATA	WR DATA
1	0	0	0	1	ERROR REGISTER	FEATURES
1	0	0	1	0	SECTOR COUNT	SECTOR COUNT
1	0	0	1	1	SECTOR NO.	SECTOR NO.
1	0	1	0	0	CYLINDER LOW	CYLINDER LOW
1	0	1	0	1	CYLINDER HIGH	CYLINDER HIGH
1	0	1	1	0	SELECT CARD/HEAD	SELECT CARD/HEAD
1	0	1	1	1	STATUS	COMMAND
0	1	1	1	0	ALL STATUS	DEVICE CONTROL
0	1	1	1	1	DRIVE ADDRESS	RESERVED

After the pattern of the CF bus cycle is known, it also needs to know the protocol of the PIO data command(In/Out), PIO non-data command which may be referenced by “ Information Technology - AT Attachment with Packet Interface Extension (ATA/ATAPI-4) Working Draft, Revision 18, 19 August 1998“ from p.223 to p.232. This protocol is used for the communication with C-Media CF flash cards that are viewed as the IDE device.

4.5 SD/MMC INTERFACE PROTOCOL

The SD/MMC communication is based on an advanced 9-pin interface (Clock, Command, Data bus and Power Line) designed to operate in a low voltage range. The both communication protocols are SD and SPI.

1. SD/MMC bus

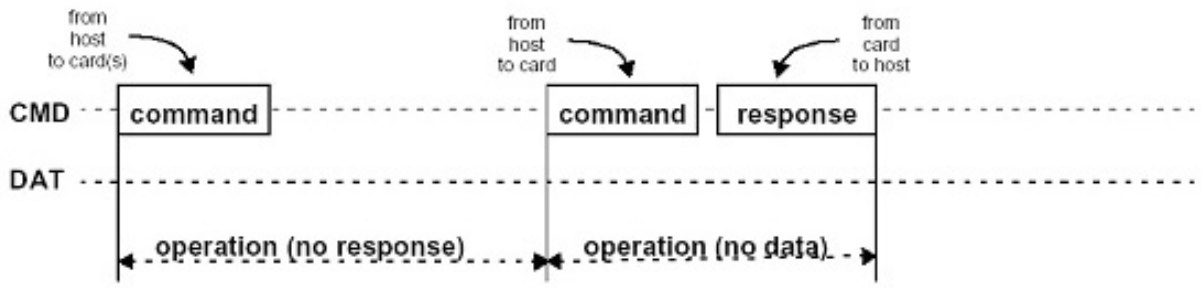


Figure 6:”no response” and “no data” operations

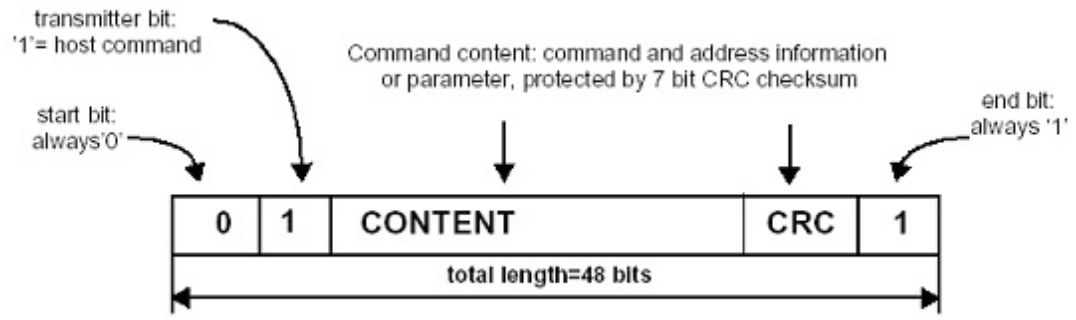


Figure 7: Command token format

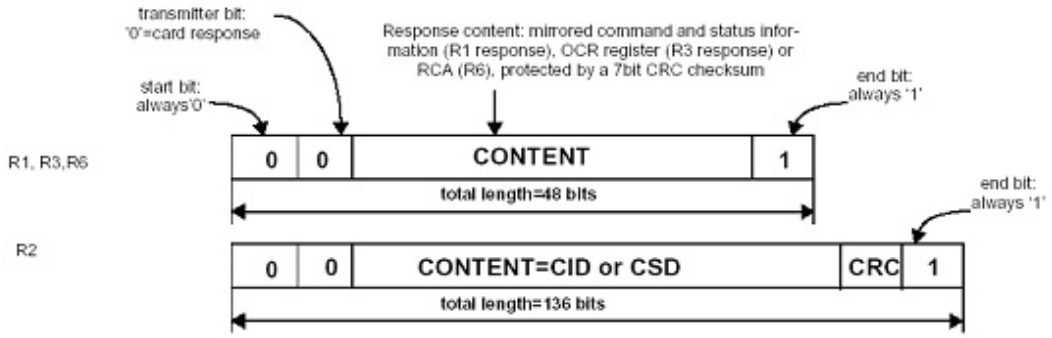


Figure 8:Response token format

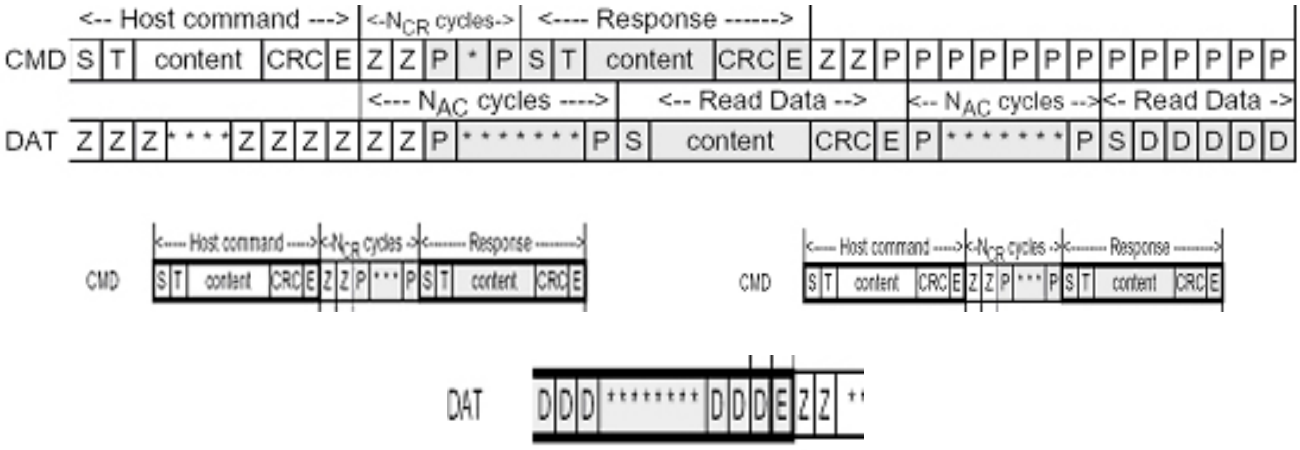


Figure 9: Timing of multiple block read command and stop command, read status command

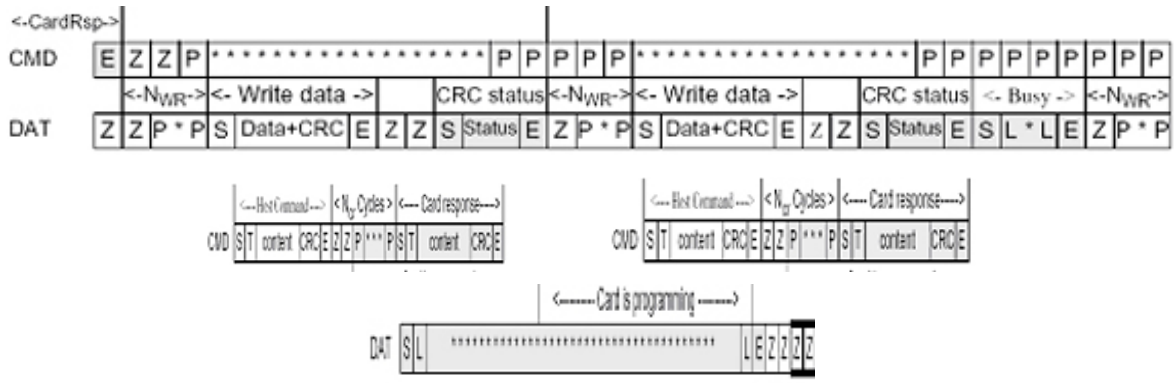


Figure 10: Timing of multiple block write command and stop command received after last data block programming, and the latter is the read status command

4.6 SM / xD INTERFACE PROTOCOL

The Smart Media / eXtreme Digital card interface provides input and output frame data streams, corresponding to the complex bundles of all digital data targeting the CM120 , and control registers.

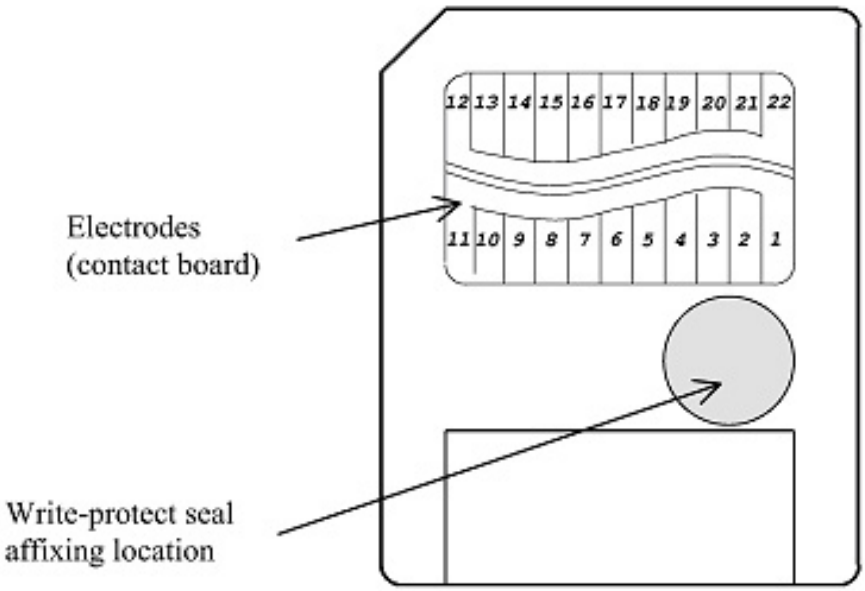
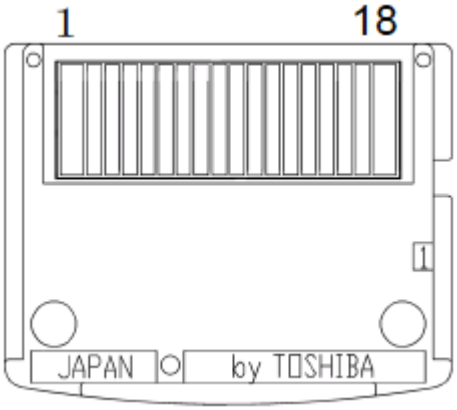


Figure 11: SmartMedia Card



Pin No.	Signals			Signal Processing		
	Pin	Type	Function	Pull Up/Down	Note	
1	GND	(O)	GND/(Card Detect)		Can double as Card Detect signal	
2	R/-B	O(OD)	Ready/Busy		2)	Open drain
3	-RE	I	Read Enable	Up	1)	
4	-CE	I	Card Enable	Up	1)	
5	CLE	I	Command Latch Enable	Down	1)	
6	ALE	I	Address Latch Enable	Down	1)	
7	-WE	I	Write Enable	Up	1)	
8	-WP	I	Write Protect	Down	1)	
9	GND		GND			
10	D0	I/O	Data0	Down		
11	D1	I/O	Data1	Down		
12	D2	I/O	Data2	Down		
13	D3	I/O	Data3	Down		
14	D4	I/O	Data4	Down		
15	D5	I/O	Data5	Down		
16	D6	I/O	Data6	Down		
17	D7	I/O	Data7	Down		
18	Vcc	S	Vcc			

S: Power supply; I: Input to Card, O: Output from Card, I/O: Bi-directional
Signal names indicate Low True signals

Figure 11.1: xD Card

4.6.1. Interface Timing Diagram Example (Smart Media / xD Card)

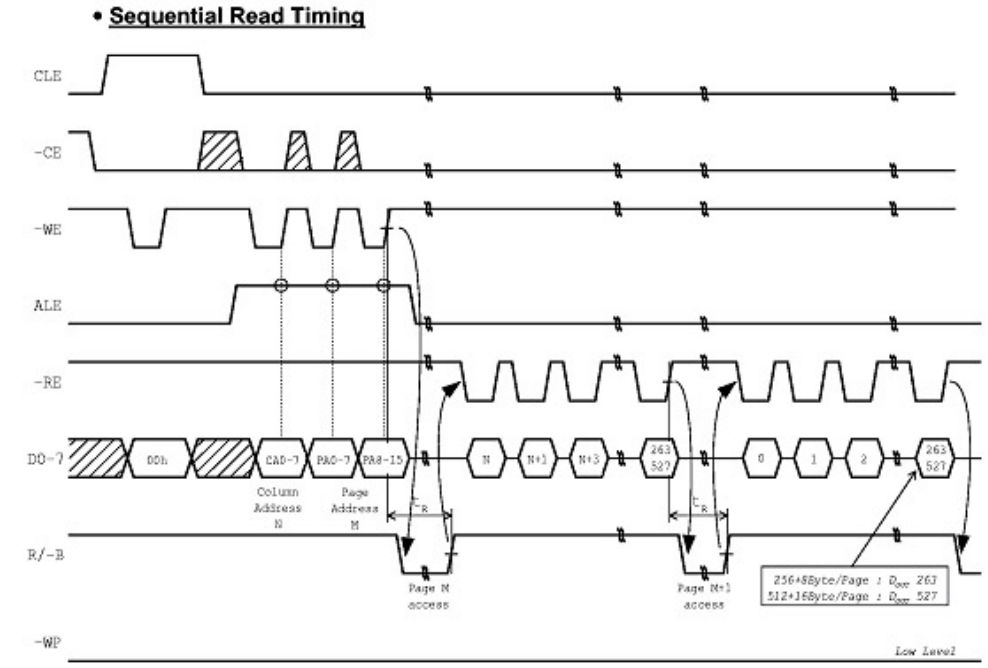


Figure 12: SM/xD Card Sequential Read Timing

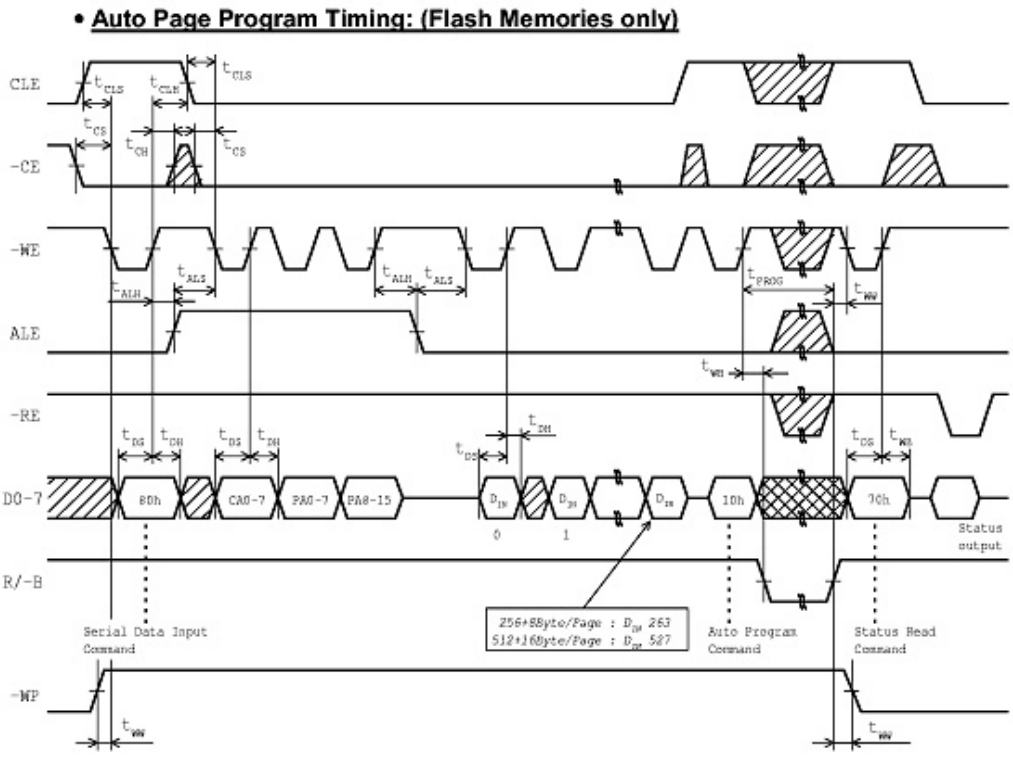


Figure 13: SM/xD Card Auto Page Program Timing

• **Auto Block Erase Timing: (Flash Memories only)**

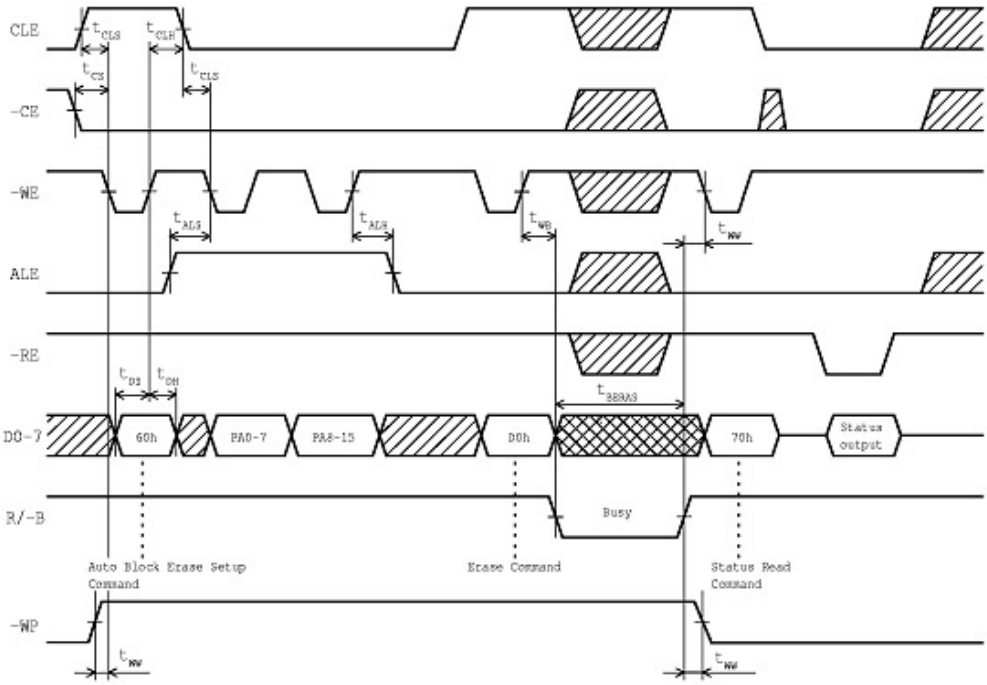


Figure 14: SM/xD Card Auto Block Erase Timing

• **ID Read Timing**

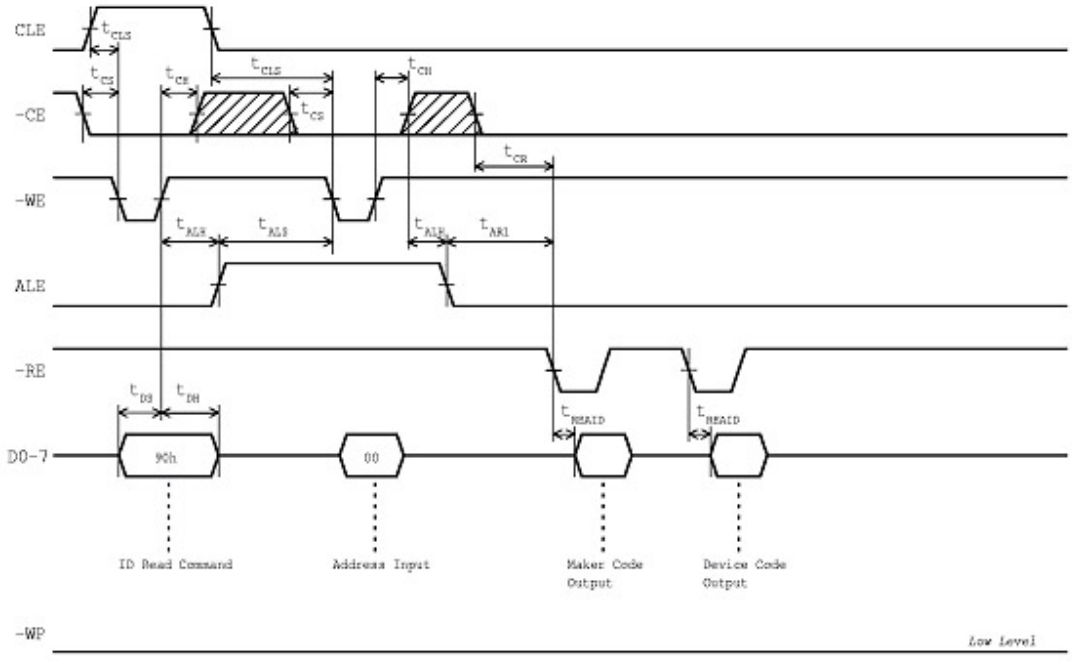


Figure 15: SM/xD Card ID Read Timing

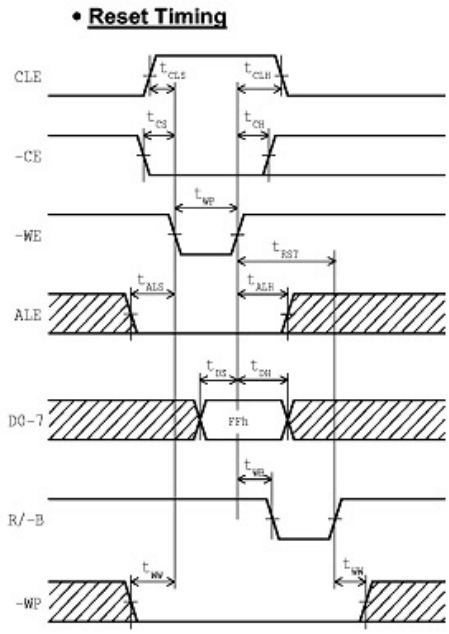


Figure 16: SM/xD Card Reset Timing

4.6.2 Description

4.6.2.1 Sequential Read

When a Data Read is executed, the initial address is specified at the start of the Data Read. Then, it is only necessary to input the –RE clock(without additional address input) in order to automatically increase the page address and continuously execute Read operation.

On the second page or the later, all data in the main and redundant sections are output using Read commands (1) and (2). Only the redundant section is output using Read command (3). The sequential Read Mode can be used only within a single block.

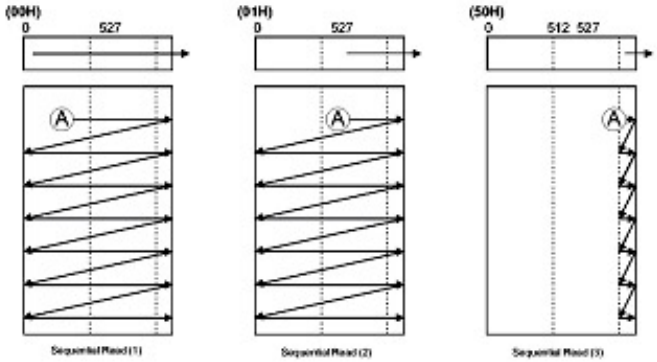


Figure 17: Sequential Read

4.6.2.2 Precautions when Programming Pages

a. Limit of the Write Operation to the Same Page
The data and redundant areas can only be written simultaneously for one time. If the system configuration requires, writing to the redundant area may occur for one more time.

b. Writing to Pages within a Block
During the program operation,writing should be executed consecutively from a lower address page to an upper address page. Random page programming should be avoided.

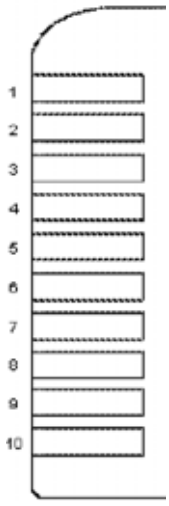
4.6.2.3 Precautions for writing in the redundant section only

Writing only to the redundant section requires the Reset command to be input and the Read command to be used to change data/pointer mode, as indicated in the following sequence.To program the data section after writing into the redundant section, the Reset command or Read commands (1) or (2) must be issued to reset the data pointer mode.

4.7 MS INTERFACE PROTOCOL

Pin Assignment

Pin No.	Pin Name
1	VSS
2	BS
3	VCC
4	DIO
5	Reserve
6	INS
7	Reserve
8	SCLK
9	VCC
10	VSS



Reverse side of the card

Serial Interface for Memory Stick:

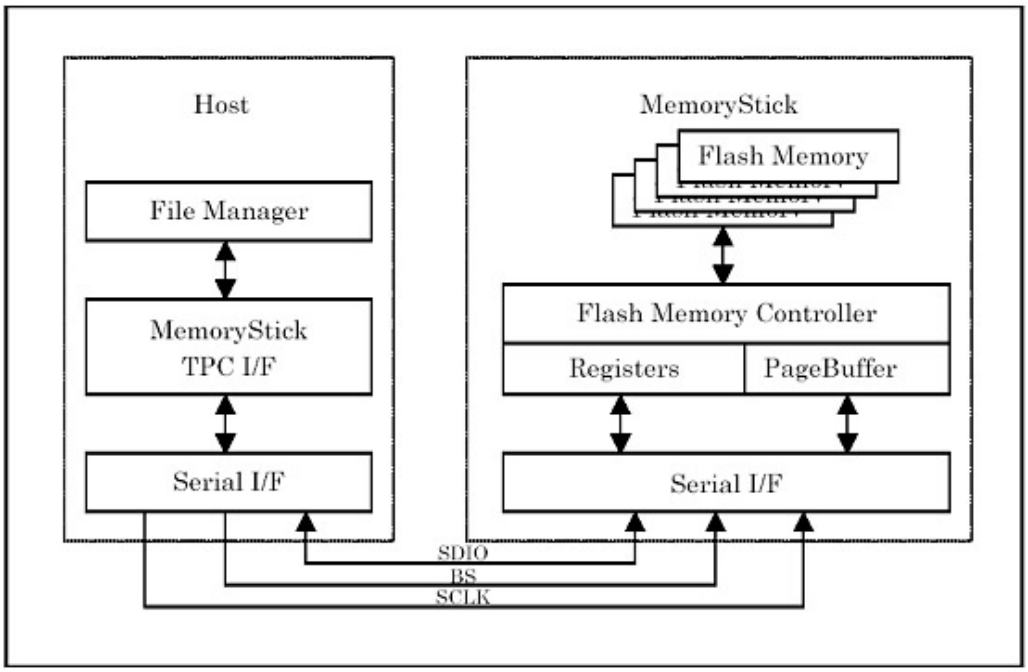


Figure 18: MS Serial Interface Block Diagram

Above is the Memory Stick block diagram. Host is on the left hand side whereas MS card on the right hand side, communicating by means of three signal lines: SDIO, BS, and SCLK. Data and command are converted on the SDIO, and regulation signals are controlled by host system via BS and SCLK. Basically, the serial interface protocol have four bus states: BS0 – IDLE stage; BS1 – TPC stage; BS2 – handshake or data stage; BS3 - handshake or data stage. Bus state sequence are different between read and write operations.

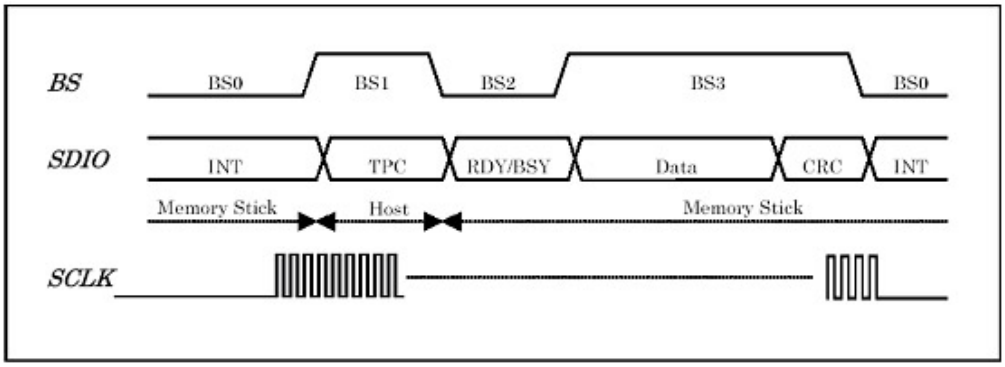


Figure 19: MS Read Protocol

Above is the MS read command running chart. It contains 4 stages: during BS1 stage, host sends the read command (all command called TPC here). During BS2 stage, MS card will tell the host if it is ready to send the data. And when data is ready, it will be sent during BS3 stage combined with 16bit CRC data. After all is done, both sides will return to BS0 stage and wait for another command or interruption.

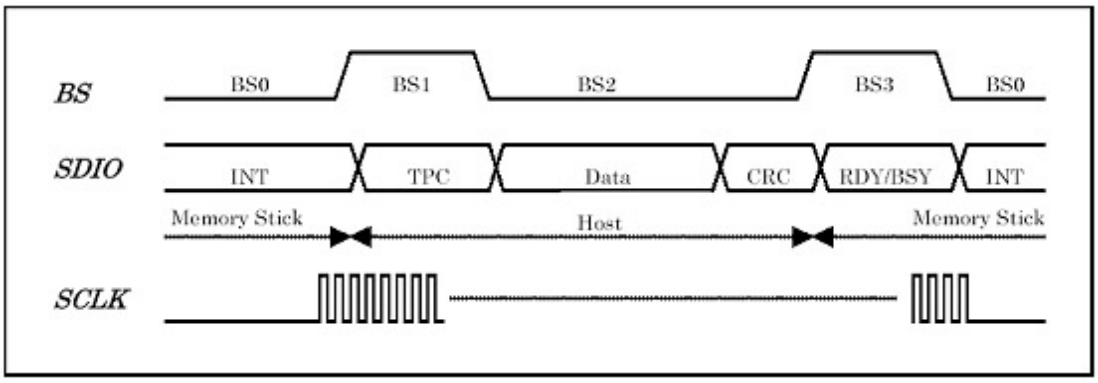


Figure 20: MS Write Protocol

Above is the MS write command running chart. Just like the read command, it contains 4 stages: BS1 stage for command to transmit from host to card. And then data will be transmitted from host to card during BS2 state with CRC check immediately. After getting the reply during BS3 stage, both sides will return to BS0 stage and wait, just like what is mentioned in the read command section.

4.8 USB LOW POWER MODE

The CM120 can be placed in the low power mode by host-issued suspend mode. Both crystal and PLL will turn off the power, and be held at a logic low power level. The CM120 USB device controller can wake up host resume signal when DP goes to low state.

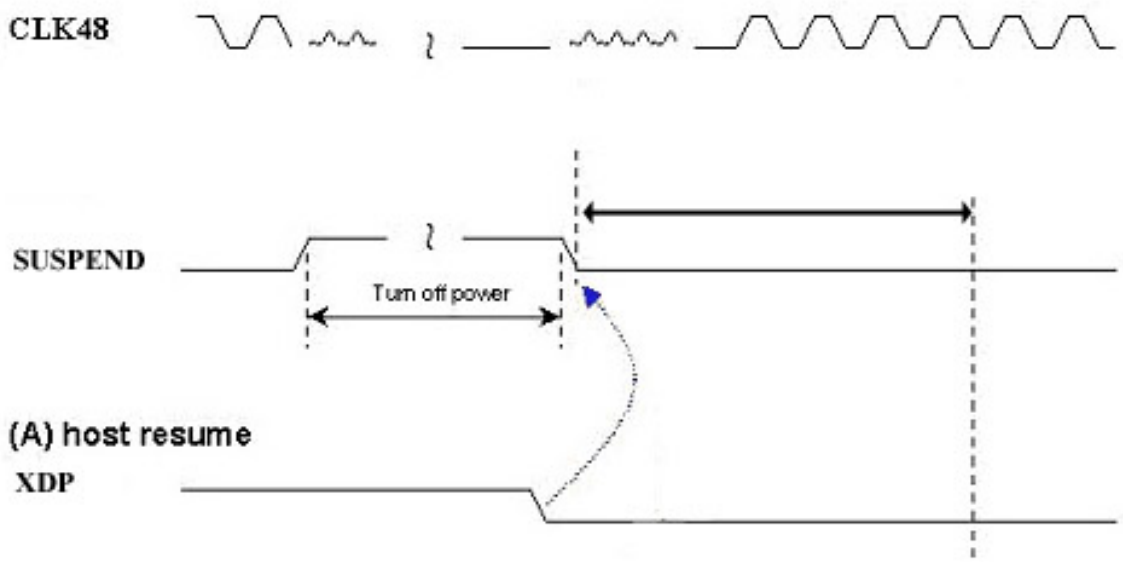


Figure 21: Suspend and Resume wakeup state

5. AC TIMING CHARACTERISTICS

(Tambient = 25 °C, AVdd = 5.0V ± 5% ,DVdd = 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

5.1 POWER-ON RESET

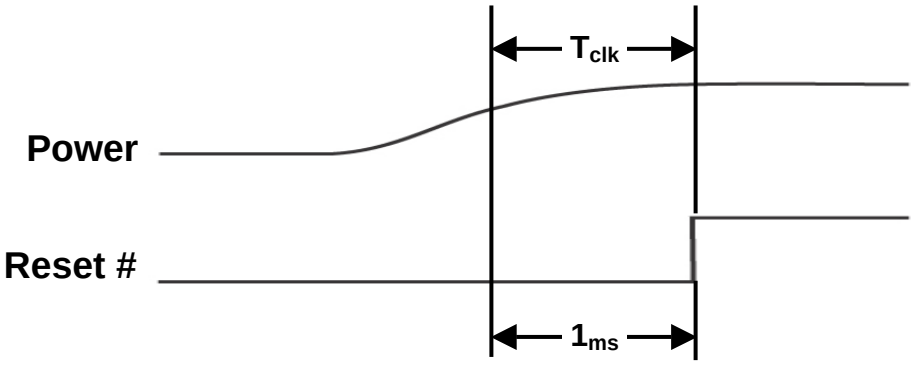


Figure 22: Power-On Reset Timing Diagram

5.2 SYSTEM RESET

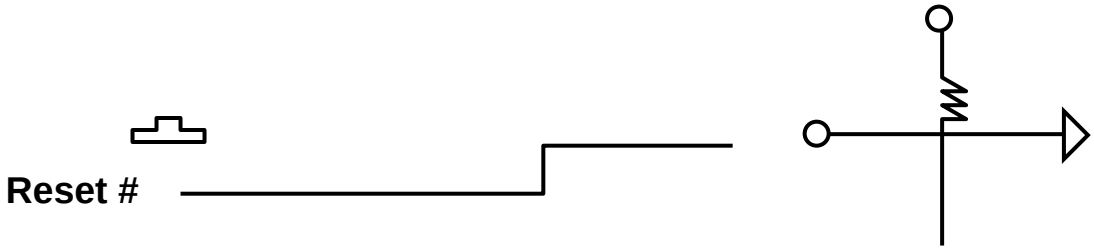


Figure 23. System Reset

5.3 CLOCKS

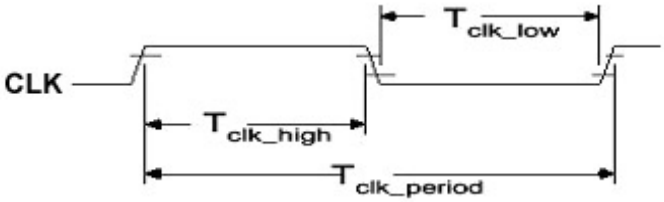


Figure 24: CLK Timing Diagram

Table 8：Clocks

Parameter	Symbol	Min	Typ	Max	Units
CLK frequency		-	12	-	MHz
CLK period	Tclk_period	-	83	-	ns
CLK output jitter		-	-	750	ps
CLK high pulsewidth (note 1)	Tclk_high	36	41.5	45	ns
CLK low pulse width (note 1)	Tclk_low	36	41.5	45	ns

Note: Worst case duty cycle restricted to 45/55.

5.4 CompactFlash Timing

Table 9：True IDE Mode I/O Input (Read) Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGLQX	0	
IORD width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note:The maximum load on –IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0 nsec, but minimum –IORD width must still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system.

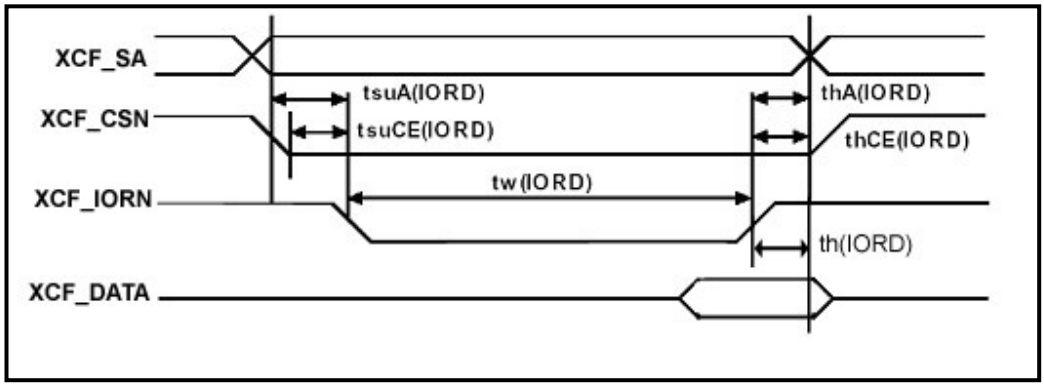


Figure 25: True IDE Mode I/O Read Timing Diagram

Table 10：True IDE Mode I/O Output (Write) Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note:The maximum load on –IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from –WAIT high to –IOWR high is 0 nsec, but minimum –IOWR width must still be met. Din signifies data are provided by the CompactFlash Storage Card or CF+ Card to the system.

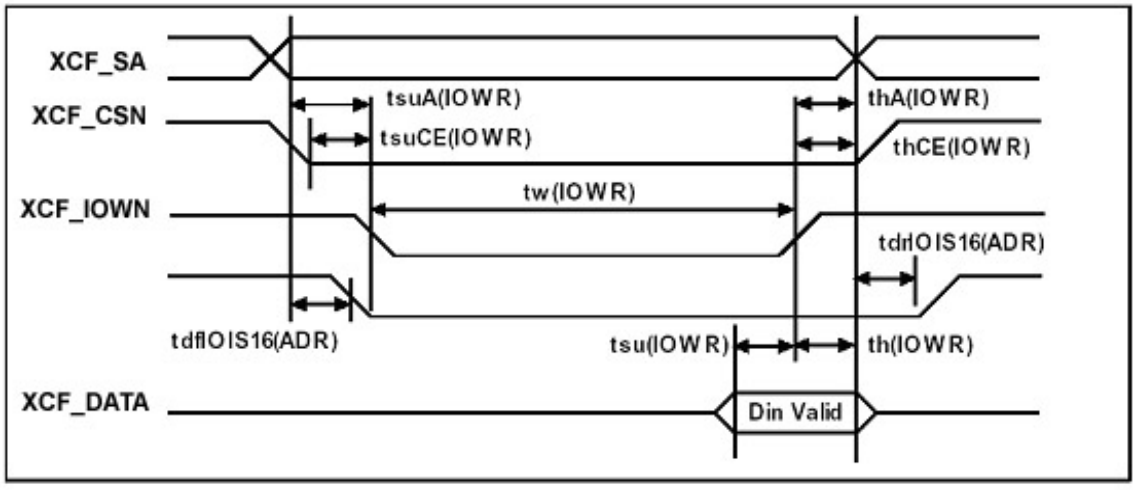


Figure 26: True IDE Mode I/O Write Timing Diagram

5.5 SECURE DIGITAL Timing

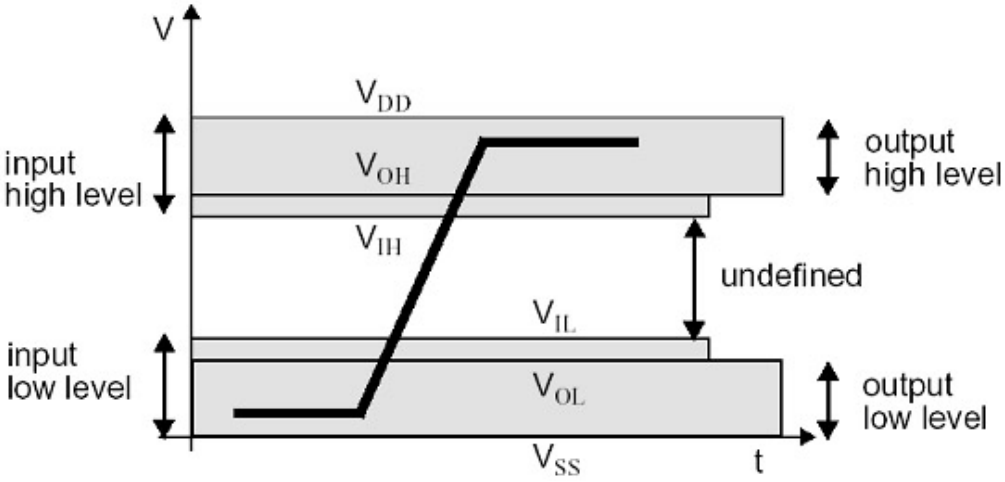


Figure 27 : SD/MMC bus signal levels

Table 11: SD/MMC bus I/O Signal Voltages

Parameter	Symbol	Min	Max.	Unit	Conditions
Output High Voltage	VOH	0.75*V_{DD}		V	1_{OH}=-100μA @V_{DD} min
Output Low Voltage	VOL		0.125*V_{DD}	V	1_{OL}=-100μA @V_{DD} min
Input High Voltage	V1H	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V1L	VSS-0.3	0.25*V_{DD}	V	

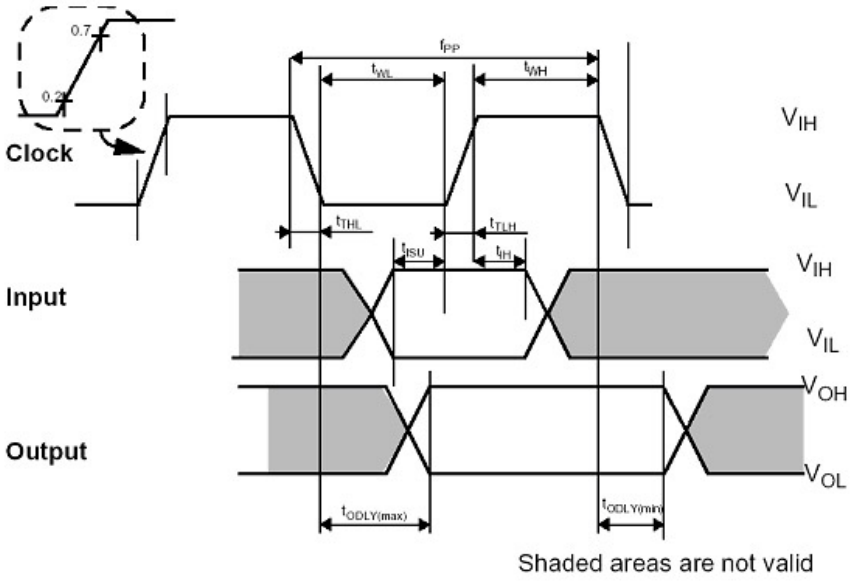


Figure 28 : Timing diagram data input/output referenced to clock

Table 12: SD/MMC Bus Timing, Parameter Value

Parameter	Symbol	Min	Max.	Unit	Remark
Clock high time	t_{WH}	50		ns	CL ≤ 250 pF (21 cards)
Clock rlse time	t_{TLH}		50	ns	CL ≤ 250 pF (21 cards)
Clock fall time	t_{THL}		50	ns	CL ≤ 250 pF (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	CL ≤ 250 pF (1 cards)
Input hold time	t_{IH}	5		ns	CL ≤ 250 pF (1 cards)
Outputs CMD, DAT (Referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	CL ≤ 250 pF (1 cards)
Clock CLK (All values are referred to min (V1H)and Max (V1L))					
Clock frequency Data Transfer Mode	f_{PP}	2	25	MHz	CL ≤ 100 pF (7 cards)
Clock frequency Identification Mode (The low freq. Si require for MultiMedia Card compatiblity).	f_{OD}	0	400	kHz	CL ≤ 250 pF (21 cards)
Clock low time	t_{WL}	10		ns	CL ≤ 100 pF (7 cards)
Clock high time	t_{WN}	10		ns	CL ≤ 100 pF (7 cards)
Clock rise time	t_{TLH}		10	ns	CL ≤ 100 pF (7 cards)
Clock fall time	t_{THL}		10	ns	CL ≤ 100 pF (7 cards)
Clock low time	t_{WL}	50		ns	CL ≤ 250 pF (21 cards)

5.6 SmartMedia Timing

5.6.1 AC Characteristics

Table 13：AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
t_{CLS}	CLE Set up Time	20	-	ns
t_{CLH}	CLE Hold Time	40	-	ns
t_{CS}	-CE Set up Time	20	-	ns
t_{CH}	-CE Hold Time	40	-	ns
t_{WP}	-WE Pulse Width	40	-	ns
t_{ALS}	ALE Set up Time	20	-	ns
t_{ALH}	ALE Hold Time	40	-	ns
t_{DS}	Data Set up Time	30	-	ns

Symbol	Parameter	Min.	Max.	Unit
t_{DH}	Data Hold Time	20	-	ns
t_{WC}	Write Cycle Time	80	-	ns
t_{WH}	-WE High Hold Time	20	-	ns
t_{WW}	-WE High to -WE Low	100	-	ns
t_{RR}	Ready to -RE Low	20	-	ns
t_{RP}	Read Pulse Width	60	-	ns
t_{RC}	Read Cycle Time	80	-	ns
t_{REA}	-RE Access Time(Serial Data Access)	-	45	ns
t_{CEH}	-CE High Hold Time(at the Last Serial Read)	250	-	ns
t_{READID}	-RE Access Time(ID Read)	-	90	ns
t_{RHZ}	-RE High to Output Hi-Z	5	30	ns
t_{CHZ}	-CE High to Output Hi-Z	-	30	ns
t_{REH}	-RE High Hold Time	20	-	ns
t_{IR}	Output Hi-Z to -RE Low	0	-	ns
t_{RSTO}	-RE Access Time(Status Read)	-	45	ns
t_{CSTO}	-CE Access Time(Status Read)	-	55	ns
t_{RHW}	-RE High to -WE Low	0	-	ns
t_{WHC}	-WE High to -CE Low	50	-	ns
t_{WHR}	-WE High to -RE Low	60	-	ns
t_{AR1}	ALE Low to -RE Low (Address Register Read,ID Read)	200	-	ns
t_{CR}	-CE Low to -RE Low (Data Register Read,ID Read)	200	-	ns
t_{WB}	-WE High to Busy	-	200	ns
t_{AR2}	ALE Low to -RE Low(Read Cycle)	150	-	ns
t_{RB}	Last -RE High to Busy(at Sequential Read)	-	200	ns
t_{CRY}	-CE High to Ready (Note)	-	1	μs

Note): The length of the period between -CE High and Ready depends on the pull-up resistance at the Ready/-Busy terminal.

5.6.2 Program/Erase/Read/Reset

During programming ,erasing, reading, or resetting operations, it is necessary to monitor the Ready/Busy status. The Busy time during the execution of each operation is shown as follows.

Table 14：Parameter

Symbol	Parameter		1MB to 128MB		Unit
			Typ.	Max.	
t_{PROG}	Program Time		-	20	ms
t_{BERASE}	Block Erase Time		-	400	ms
t_R	Data Transfer Time (from Cell to Register)		-	100	μs
t_{rst}	Device Resetting Time (Program/Erase/Read)	Program	-	80	μs
		Erase	-	6	ms
		Read	-	40	μs

(Note): For details, see each company's technical data.

5.7 xD Timing

5.7.1 AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
t_{CLS}	CLE Setup Time	20	-	ns
t_{CLH}	CLE Hold Time	40	-	ns
t_{CS}	-CE Setup Time	20	-	ns
t_{CH}	-CE Hold Time	40	-	ns
t_{WP}	-WE Pulse Width	40	-	ns
t_{ALS}	ALE Setup Time	20	-	ns
t_{ALH}	ALE Hold Time	40	-	ns
t_{DS}	Data Setup Time	30	-	ns
t_{DH}	Data Hold Time	20	-	ns
t_{WC}	Write Cycle Time	80	-	ns
t_{WH}	-WE High Hold Time	20	-	ns
t_{WW}	-WP High to -WE Low	100	-	ns
t_{RR}	Ready to -RE Low	20	-	ns
t_{RP}	Read Pulse Width	60	-	ns
t_{RC}	Read Cycle Time	80	-	ns
t_{REA}	-RE Access Time	-	45	ns
t_{CEA}	-CE Access Time	-	55	ns
t_{CEH}	-CE High Hold Time(at the Last Serial Read)	100	-	ns
t_{OH}	Output Data Hold Time	10	-	ns
t_{RHZ}	-RE High to Output Hi-Z	-	30	ns
t_{CHZ}	-CE High to Output Hi-Z	-	20	ns
t_{REH}	-RE High Hold Time	20	-	ns
t_{IR}	Output Hi-Z to -RE Low	0	-	ns
t_{RHW}	-RE High to -WE Low	0	-	ns
t_{WHR}	-WE High to -RE Low	50	-	ns
t_{AR1}	ALE Low to -RE Low(ID Read)	100	-	ns
t_{AR2}	ALE Low to -RE Low (Read Cycle)	50	-	ns
t_{CR}	-CE Low to -RE Low(ID Read)	100	-	ns
t_{WB}	-WE High to Busy	-	200	ns
t_{RB}	Last -RE High to Busy(at Sequential Read)	-	200	ns
t_{CRY}	-CE High to Ready (Note)	-	$6+t_r$(RY/-BY)	µs

Note: The time required to go from -CE High to Ready depends on the pull-up resistance applied to the Ready/-Busy pin.

5.7.2 Program/Erase/Read/Reset

Symbol	Parameter		16 MB - 2 GB			Unit
			Min.	Typ. (Note)	Max.	
t_{PROG}	True Program Busy Time		-	(200)	1000	µs
t_{BERASE}	Block Erase Busy Time		-	(2)	10	ms
t_{DBSY}	Dummy Program Busy Time during Multi Block Programming		0.5	(2)	10	µs
t_{MBPBSY}	Multi Block Program Busy Time		-	(200)	1000	µs
t_R	Data Transfer Time (from Cell to Register)		-	-	25	µs
t_{rst}	Device Resetting Time (Program/Erase/Read)	Program	-	-	20	µs
		Erase	-	-	0.5	ms
		Read	-	-	6	µs

Note: Details are in the suppliers data sheet.

5.8 MemoryStick Timing

Table 15 : ATE Test Mode Timing

Signal	Parameter	Standards		Unit
		Min	Max	
SCLK	Cycle	50		ns
	H Pulse Time	15		ns
	L Pulse Time	15		ns
	Rise Time		10	ns
	Fall Time		10	ns
BS	Setup Time	5		ns
	Hold Time	5		ns
DATA	Setup Time	5		ns
	Hold Time	5		ns
	Output Delay		15	ns

6. REFERENCES

—End of Specifications—

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E-mail：sales@cmedia.com.tw URL：http://www.cmedia.com.tw