Evaluation about Solder-IMC Crack of Fine Pitch BGA Package

Taeho Kang, Ara Lee, Jaewoo Jeong, Dongok Kwak
Samsung Electronics
1-1,Samsungjeonja-ro
Hwaseong-si,Gyeonggi-do 445-701 Korea
taeho0526.kang@samsung.com

Abstract

FBGA is widely adopted as AP and memory package for mobile devices such as a smart phone and a smart watch. FBGA is attached to PCB assembly during SMT process. Double side SMT is preferred to increase the battery area for slim design and long life of mobile device. Solder-IMC crack is in-process reliability failure occurs during 2nd side SMT. The buried via is often used in double side SMT PCB is filled with filler material of CTE is highly mismatched to surrounding PCB laminates (FR-4). Tensile stress is applied to BGA pad by this CTE mismatch at high temperature and causes the solder-IMC crack. In this paper, we evaluate the factors of solder-IMC crack related to PCB and BGA. It is found that the length of buried via related to PCB thickness influences the solder-IMC crack. But if the location of buried via is not aligned to the location of BGA pad, solder-IMC crack does not occur. In the case of buried via and BGA pad are aligned each other, the failure rate of solder-IMC crack can be lowered by controlling O_2 level that is less than 1000ppm and by applying solderball with high Ag content for SAC alloy. The temperature cracking solder-IMC interface is measured. The result shows that the solder-IMC crack occurs before solder joints are fully melted. The solder joint with low Ag content having broad melting temperature range is relatively weaker than high Ag having near eutectic point. It is recommended to design the PCB with buried via which avoids the location of the BGA pad and this is the good solution to reduce the failure rate of solder-IMC crack to near zero.

Key words

CTE mismatch, buried via, FBGA, solder-IMC crack, solder joint reliability

I. Introduction

Fine pitch BGA (FBGA) is widely used as AP, memory IC package in mobile market because of its good properties such as area-saving, thin thicnkess, light weight and large pin count. Array of solderballs is placed at the bottom of BGA substrate and is connected to the surface of PCB by surface mount technology (SMT). For mobile device, double side SMT is preferred to extend the battery area to increase usability and for more convenience. During SMT process, the solderball attached to package melts in the reflow chamber heated above the melting temperature and bonds naturally to pad metal of PCB forming IMC composed of Sn, Ag, Cu and the others. Sometimes poor solder joint such as a head in pillow, a tombstone and a solder bridge occurs according to its process condition. Even though there is not an initial soldering failure at all, it is possible to degenerate solder joint of 1st side to crack during 2nd side SMT [1]. The crack occurs between solder and IMC but the crack interface of IMC and solder does not match each other as shown in Fig.1. This solder joint crack is different from the well-known reliability failure by drop test and TC test [2]-[4]. In former research, the solder-IMC crack turned out that the CTE mismatch by buried via filler is a major factor. We further evaluate the solder degeneration mechanism by buried via and the related factors depending on package design.

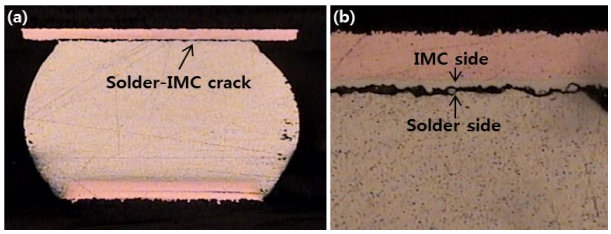

Fig.1. Cross sectional view of solder-IMC crack.

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II. Solder-IMC crack

We reviewed the estimated mechanism of solder-IMC crack as shown in Fig.2. Solder-IMC crack occurs during 2nd side SMT and the driving force is caused by CTE mismatch between buried via filler and PCB laminates (FR-4).

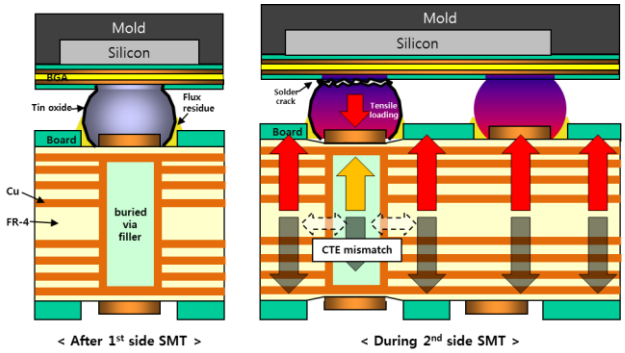

Fig.2. Estimated mechanism of solder-IMC crack.

A. *Solder-IMC cracking during 2nd side SMT*

The Solder-IMC crack occurs only at 2nd side SMT. SMT process flows from solder paste printing, component pick&place to reflow. Solder paste is made up of small particle of solder alloy and flux. The flux is activated to remove tin oxide layer of solderball and improve wetting to metal pad during 1st side SMT and then remains as residue lost its function. As a result of 1st side SMT, a number of solder joint is formed and thin tin oxide layer is formed naturally at surface of the solder joint. During 2nd side SMT, the solder joint that already exists is exposed to reflow temperature above melting temperature but is not fully melted again because the flux is not activated and the tin oxide of joint surface is still remained [5]. It is expected that the tin oxide layer of joint surface influences the solder-IMC crack mechanism.

B. *Driving force*

The driving force of solder-IMC crack is a relative contraction force driven by z-axis CTE mismatch between buried via filler and laminates (FR-4) of PCB. CTE of buried via filler is normally about 30~40ppm below Tg and about 100~150ppm above Tg depending on its vendor. Z-axis CTE of FR-4 is normally about 40~60ppm below Tg and about 230~280ppm above Tg depending on its vendor. CTE difference of these materials above Tg is large and the PCB surface above buried via expands along z-axis less than PCB surface surrounding buried via as temperature ramps up to peak reflow temperature. Thus the solder joint on the BGA pad above buried via experiences tensile stress and is finally detached from metal pad cracking solder-IMC interface. The side wall of solder joint is covered with tin oxide but inside of solder joint is melted around peak temperature. Thus it can be suggested that the solder joint is hard enough to withstand relative contraction of buried via filler at the moment of solder-IMC crack. It is expected that the solder-IMC crack occurs before the solder joint is fully melted.

III. Experiment

We designed several experiment to crack the solder joint interface by CTE mismatch between buried via filler and FR-4. We did SMT using various designs of PCB and BGA and then we analyzed joint failure rate using destructive methods such as detach, X-section and dye&pry test. We only counted the solder-IMC crack excluding the crack within IMC and bulk and pad lift. The interface of solder-IMC crack does not match each other, and also morphology of IMC is different from the solder joint failure of drop and TC test [2]-[4]. In our SMT process, 11.5x13mm^2-size FBGA with SAC alloy solderball, 132x77mm^2-size JEDEC PCB with buried via, Koki S3X58-M-301-4 solder paste and 80um thick stencil mask are used. All metal pads are Cu-OSP. Peak temperature of reflow chamber sets up 260 degree Celsius and dwell time above 218 degree Celsius is within 60 seconds.

A. *DOE #1 – PCB, BGA specification with reflow condition*

In DOE #1, we experimented solder joint crack rate depending on PCB thickness with different buried via length, BGA thickness, solderball with different Ag content and reflow condition. DOE#1 Matrix is shown at Table.1.

PCB parameter	BGA parameter		reflow condition
Thickness (buried via length)	Thickness	Solderball composition	
1.2 mm (0.6mm)	0.8 mm	SAC/Low Ag	N2 purge (O2 < 1000ppm)
1.5 mm (1.0mm)	1.0 mm	SAC/High Ag	Air
	1.2 mm		

Table.1. DOE Matrix #1.

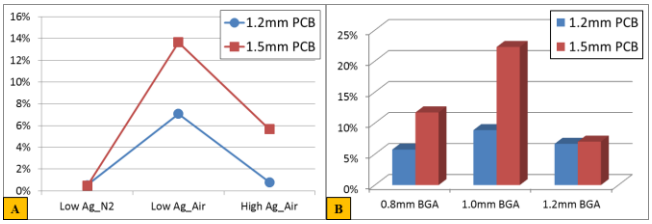

Fig.3. Comparison of solder joint failure rate according to (a) PCB thickness, reflow condition, (b) PCB and BGA thickness for low Ag, air reflow case.

The solder-IMC cracking rate from DOE #1 is shown in Fig.3. The failure rate is influenced by O_2 level of reflow chamber (N_2 purge) and the thickness of PCB related to the

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length of buried via. The generation of tin oxide layer of solder joint is suppressed by controlling O_2 level less than 1000ppm. Thus tin oxide layer has a negative influence on solder joint. The thickness of BGA does not have an influence on failure rate. The result based on Ag content of Fig.3(a) show us that drastic reduce of failure rate as Ag content goes higher. As Ag content is higher, Solderball of SAC alloy melts at lower temperature and has stronger bulk strength [6]-[8]. Lower melting temperature means that the BGA pad is under lower tensile stress because FR-4 is less expanded at lower temperature and also high Ag content solder joint may melt before the tensile stress increases enough to cause solder-IMC crack.

B. DOE #2 – the location of buried via

In DOE #2, we experimented with the occurrence of solder-IMC crack according to location of buried via. Solder-IMC crack is caused by buried via beneath BGA pad. The PCB is designed as shown in Fig.4(a). As shown in Fig.4(b), PCB is designed with various locations of buried via and the BGA is mounted at the same time to compare the failure rate in the same reflow chamber condition. For all cases as shown in Table.1, there were not a solder-IMC crack for the design of buried via between 4 pads and 2 pads. The solder-IMC crack occurs only at the BGA pad above buried via. It is recommended to design the buried via avoiding BGA pad.

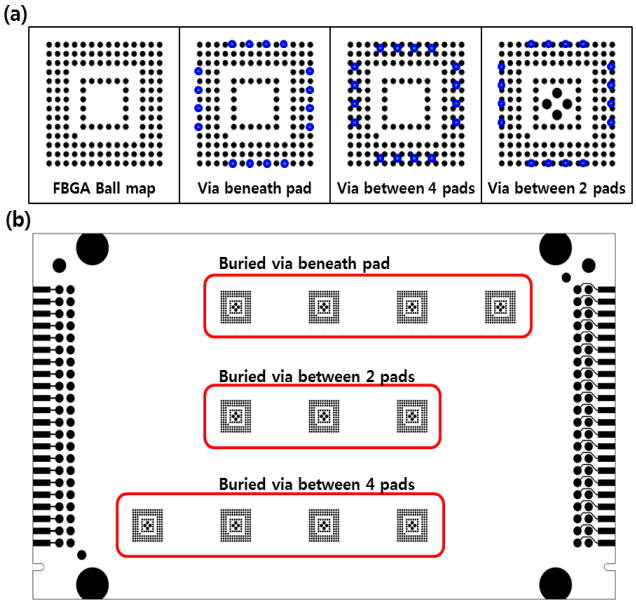

Fig.4. (a) Buried via (blue circle) design of PCB, (b) buried via designed JEDEC PCB divided by 3 groups (beneath pad, between 4 pads, between 2 pads).

In addition, we experimented with influence of the solder-IMC crack according to local warpage of BGA. The count of buried via is increased more than previous experiment as shown in Fig.5(a). The contour plot of BGA is shown in Fig.5(b) according to measuring temperature. The warping behavior of BGA top and left side is different each other. The warpage of top side is larger than left side. Fig.5(c) is a result of dye&pry test. Fig.5(d) shows the accumulated result of dye&pry test failure at each pad above buried via and shows that total count of left side and top side is similar, 63 and 65. Accordingly the warping behavior of BGA does not have an influence on the failure.

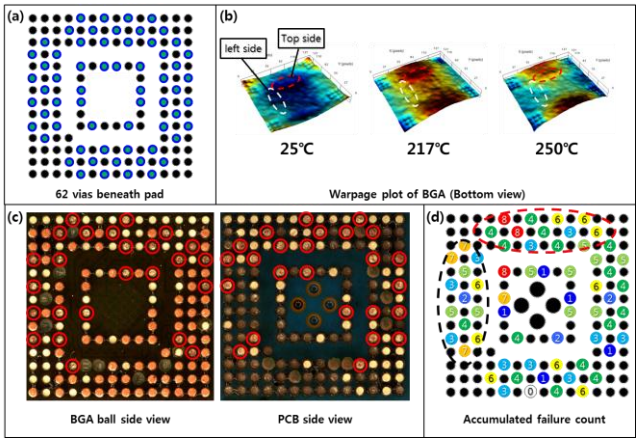

Fig.5. (a) Buried via(blue circle) design of PCB, (b) contour plot of BGA warping behavior depending on temperature, (c) result of dye&pry (red circle : solder-IMC crack), (d) accumulated dye&pry test failure count of solder-IMC crack for each pad above buried via.

C. DOE #3- the temperature in which the crack occurs

In DOE #3, we tried to find out about the difference according to Ag content and measure the temperature in which the solder-IMC crack occurs. In this experiment, heater block, thermometer and bond tester (Dage-4000Plus) are used as shown at Fig.6. Tensile stress is applied to solder joint by pushing the PCB. As bond tester pushes the backside of PCB, the solder joint at the edge of BGA undergoes the tensile stress similar to relative contraction of buried via. We measured the joint cracking temperature with the high Ag and low Ag content of solder joint.

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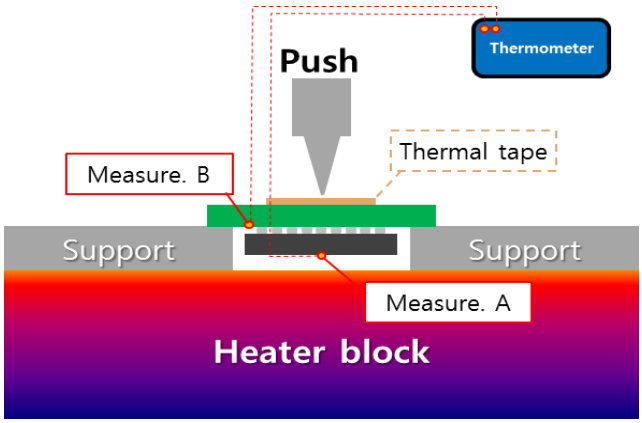

Fig.6. Experimental setup to measure temperature cracking solder-IMC interface.

The setting temperature of heater block is listed at Table.2. The temperature of BGA topside (A) and PCB topside (B) is monitored and a real temperature of solder joint is estimated by averaging the temperature of monitoring spot after push. After applying tensile stress, the BGA is detached to verify whether the solder-IMC crack occurs. The result shows that solder-IMC crack occurs within some temperature range before melting point of solder joint. For the low Ag content solder joint, solder-IMC crack and collapsed solder joint by melting occur simultaneously at setting temperature 270 degree Celsius. The reason is considered that real joint temperature differs locally and is close or above its melting temperature. Because the low Ag solder joint has broader melting temperature range by two distinct melting phases than that of the high Ag solder joint, it is possible for the low Ag content solder joint to crack solder-IMC interface at higher temperature than near eutectic point of high Ag content [7]. Thus solder joint with low Ag content is relatively weak to be cracked at the solder-IMC interface.

Seting Temperature	Estimated joint Temperature	SAC / Low Ag	SAC / High Ag
240	198.5	No fail	No fail
250	205	No fail	Solder-IMC crack
260	215	Solder-IMC crack	Solder-IMC crack
270	220	Solder-IMC crack	Melting
		Melting	

Table.2. The estimated joint temperature in which the solder-IMC crack occurs

IV. Conclusion

Solder-IMC crack is in-process reliability failure by tensile stress applied to metal pad of PCB and BGA substrate during 2nd side SMT. Tensile stress is caused by the CTE mismatch between buried via filler and PCB laminates (FR-4) as reviewed. It is evaluated that what is major parameter causing solder-IMC crack in view of PCB and BGA design. It is found that the length of buried via related to PCB thickness influences the failure rate of solder-IMC crack. Also it is found that the solder-IMC crack failure rate can be lowered by applying low O_2 level during SMT process and solderball with high Ag content. We experimented to find out the reason of different failure rate by applying tensile stress on metal pad directly and by measuring the temperature of PCB and BGA. The result shows that solder-IMC crack occurs before the solder joint is fully melted and this is the reason why solder joint with low Ag content is relatively weaker than high Ag because of broad melting temperature range.

FBGA with low Ag solderball is preferred because of its outstanding reliability of drop test. But low Ag content is a relatively weak soldering in the aspect of SMT process. With well-known phenomena such as Non-wet and head in pillow, it is recommended to consider the condition that causes the solder-IMC crack. Best recommendation for preventing solder-IMC interface from cracking is to design buried via, avoiding the location of the BGA pad. If it is impossible to avoid, it is recommended to apply the SMT reflow chamber with O_2 level less than 1000ppm and the solderball with high Ag content. Even though it shows low failure rate of solder-IMC crack as shown in our experiments, it is close to zero ppm but not zero in the aspect of mass production.

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