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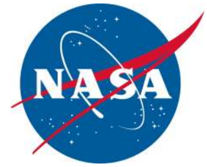

NASA Guidelines for Ball Grid Array (BGA) and Die-Size BGA (DSBGA) Selection and Application

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NASA Electronic Parts and Packaging (NEPP) Program

Office of Safety and Mission Assurance

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OBJECTIVES AND PRODUCTS

This guideline document presents recommendations for use of advanced plastic ball grid array (BGA) and die-size BGA (DSBGA)—commercial-off-the-shelf (COTS)—packaging technologies and assemblies for high-reliability applications. The most advanced and high-density BGAs come in the flip-chip ball grid array (FCBGA) configurations with inputs/outputs (I/Os) of more than 2000 with 1 mm pitch. DSBGAs with lower than 1 mm pitch—as low as 0.3 mm pitch, generally have a maximum of a few hundred I/Os. Due to the yield challenges of larger die and the high cost of node shrinkages, industry has moved towards the implementation of System in Package (SiP). Advanced SiP integrated die technologies, known as Chiplets, are the next paradigm shift in electronics packaging technologies. This guideline includes a brief discussion on advanced COTS packaging technology trends with two test evaluation examples; one for BGAs and the other for DSBGAs. For the two categories, test results are presented covering the key process issues, quality indicators, and quality assurance (QA) control parameters followed with a comprehensive test data to address thermal cycle reliability and limitations. Finally, key recommendations derived from the lessons learned during these evaluations are included in the report summary. Specific recommendations of COTS BGAs/DSBGA packaging technologies were given for low risk infusion spaceflight applications with consideration of Mission, Environment, Applications, and Lifetime (MEAL) requirements.

Key Words: COTS, commercial-off-the-shelf, Ball grid array, BGA, FCBGA, chip scale package, CSP, die-size ball grid array, wafer level package, WLP, CVBGA, LGA, solder joint reliability, thermal cycle

TABLE OF CONTENTS

1 BGA/DSBGA PACKAGING TECHNOLOGIES ... 1-1
1.1 Packaging Trends: BGAs to DSBGAs ... 1-1
1.2 BGA Packaging Technologies ... 1-1
1.2.1 Advantages of BGAs ... 1-2
1.2.2 Disadvantages of BGAs ... 1-3
1.3 DSBGA Packaging Technologies ... 1-4
1.4 Guideline Limitations ... 1-5
2 BGA/FCBGA ASSEMBLIES UNDER THERMAL CYCLING ... 2-1
2.1 Test Matrix ... 2-1
2.2 Package Styles ... 2-1
2.3 PCB Design and Surface Finish ... 2-3
2.4 Limitation of HASL Finish for BGA and ENEPIG for DSBGA ... 2-3
2.5 Assembly Parameters for a Mixed BGA & DSBGA ... 2-4
2.6 Optical Inspection after Assembly ... 2-5
2.7 BGA X-ray Characterization after Assembly ... 2-6
3 BGA THERMAL CYCLES (–55/100°C OR –65/150°C) ... 3-1
3.1 BGA Thermal Cycles (–55°C /100°C) ... 3-1
3.2 BGA Thermal Shock Cycle (–65°C /150°C) ... 3-3
4 DSBGA ASSSEMBLIES UNDER THERMAL CYCLES ... 4-1
4.1 Test Matrix ... 4-1
4.2 Package Styles ... 4-2
4.3 Assembly and Inspection Processes ... 4-3
4.4 ASSEMBLY PROCESSES MODIFICATION REQUIRED ... 4-5
5 DSBGA THERMAL CYCLE AND FAILURE ANALYSIS TEST RESULTS ... 5-1
5.1 Thermal Cycle Profile ... 5-1
5.2 Thermal Cycle Test Results/Discussion for CC80 ... 5-1
5.3 Thermal Cycle Test Results/Discussion for eWLP-LGAs ... 5-2
5.4 Thermal Cycle Test Results/Discussion for CV-LGA and CVBGA ... 5-4
6 NASA APPLICATION: BGA/DSBGA ... 6-1
6.1 Purpose and Recent Findings on COTS ... 6-1
6.2 Missions & BGA/DSBGA Applications ... 6-2
6.3 BGA/DSBA Package Construction Review ... 6-4
6.4 BGA/DSBGA PCB Assembly ... 6-6
6.5 BGA/DSBGA for MEAL ... 6-8
6.6 MEAL BGA/DSBA Assembly Testing ... 6-9
6.7 Non-traditional Testing: HALT/HASS for BGA/DSBGA ... 6-11
7 SUMMARY ... 7-1
8 ACRONYMS AND ABBREVIATIONS ... 8-1
9 REFERENCES ... 9-1

1 BGA/DSBGA PACKAGING TECHNOLOGIES

1.1 PACKAGING TRENDS: BGAS TO DSBGAS

Ball grid arrays (BGAs) and die-size BGAs (DSBGAs), also called chip scale packages (CSPs), are widely used for numerous electronics applications, including portable and telecommunication products [1-4]. BGAs with 1.27 mm pitch and 1000 I/Os or fewer are used for high-reliability applications that generally demand more stringent thermal-cycling and mechanical loading requirements. Industry adopted two key methods to increase the density of a single device and package, subsequently adding the third stacking dimension. For a single package, the I/Os are continuously increasing. Plastic BGAs (PBGAs) with 1.0 mm pitch and more than 2000 I/Os are now offered by package suppliers.

The higher I/O PBGAs come in the flip-chip die version (FCBGA). PBGAs were introduced in the late 1980s, were implemented with great caution in the early 1990s, and evolved into various DSBGAs with much finer pitches of 0.3 mm and thinner configurations. Scaling at the package level rather than at the die level (Moore's Law) through pitch, and integrating more functions in a package reduces cost and time to market due to recent scaling limitations and node reduction at the die level. This caused an explosion in packaging technologies as shown in Figure 1-1 [5].

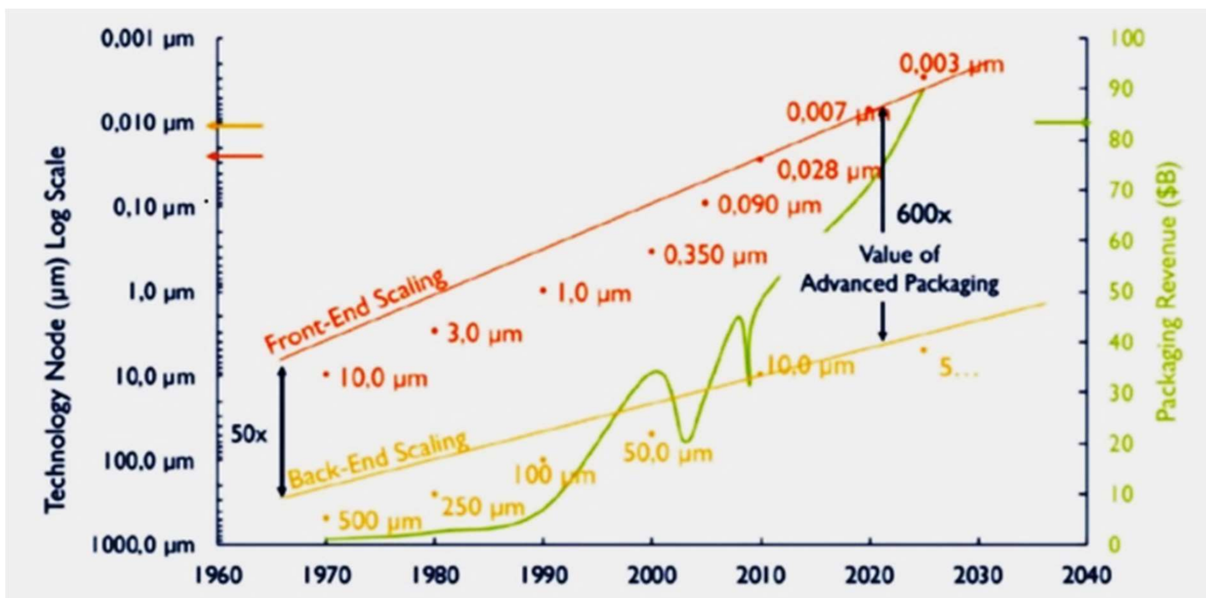

Figure 1-1. Die level (Front-End) scaling versus package level (Back-End) plots showing explosion in advanced packaging technologies in the last decade [5].

1.2 BGA PACKAGING TECHNOLOGIES

In general, the tin-lead version of area arrays come in many different package styles, including the COTS ball grid array (BGA) with ball composition of eutectic Sn63Pb37 alloy, or slight variations such as Sn60Pb40. As the commercial industry transitions to the restriction of hazardous substances (ROHS), the availability of advanced PBGA packages with tin-lead balls will become rare. It is

therefore desirable to also include BGA packages with Pb-free solder balls for evaluation. The higher I/O PBGAs come in the flip-chip die version.

As shown in Fig. 1-2, the flip-chip BGA (FCBGA) is similar to the BGA, except that an internal flip-chip die is used rather than a wire-bonded die. For BGAs with more than 600 I/Os, FCBGAs are used in order to accommodate the larger number of I/Os required for the flip-chip die within the FCBGA package (see Figure 1-3). Compared to quad-flat pack (QFP), area array accommodates extremely high I/O counts and provides improved performance. BGAs also provide improvement in electrical and thermal performance, more effective manufacturing, and ease of handling compared to conventional surface mount (SMT) leaded parts.

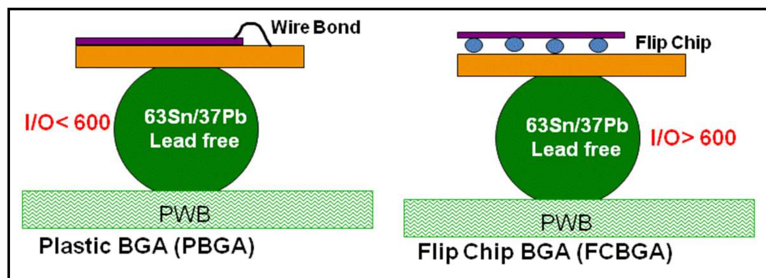

Figure 1-2. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high I/O package configurations, respectively. Most solder balls now come in lead-free rather than tin-lead.

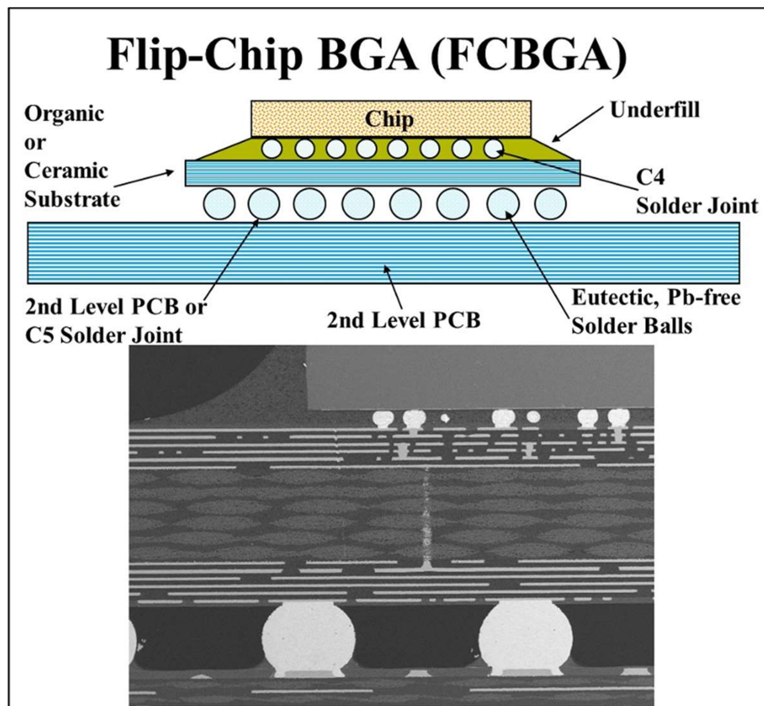

Figure 1-3. Schematic drawing for Flip-Chip BGA (FCBGA) and a X-section of FCBGA.

1.2.1 *ADVANTAGES OF BGAS*

Area-array packages offer several distinct advantages over fine-pitch surface mount components with gull wing leads, including:

- High I/O capability (hundreds to approximately 3000 balls can be built and manufactured, but QFPs are limited to less than 300 I/Os).
- Higher packaging densities. This is achievable because the limit imposed by package periphery for the QFP is not applicable in the case of area array packages. Area rather than periphery is used. Hence, it is possible to mount more packages per the same board area.
- Faster circuitry speeds than QFP surface mount components (SMCs) because the terminations are much shorter and therefore less inductive and resistive.
- Better heat dissipation because of more connections with shorter paths.
- Easier assembly processes than those required for conventional SMT manufacturing and assembly technologies such as stencil printing and package mounting.

Standard COTS BGAs are also robust in processing. The robustness stems from their higher pitch (typically, 0.8–1.27 mm), better lead rigidity, and self-alignment characteristics during reflow processing. The latter feature, self-alignment during reflow (attachment by heat), is very beneficial and opens the process window considerably. Note, however, that the manufacturing robustness decreases with decreases in pitches. Assembly is particularly challenging for 0.4 mm and 0.3 mm pitches, especially in the vicinity of a larger pitch PBGAs and SMCs.

1.2.2 *DISADVANTAGES OF BGAS*

Area array packages are not compatible with multiple solder processing methods, and individual solder joints cannot be visually inspected and reworked using conventional methods. For high-reliability SMT assembly applications, the ability to inspect the solder joints visually is a standard inspection requirement and is a key factor for providing confidence in solder joint reliability. Industry has continuously developed advanced inspection techniques, including X-ray, to improve inspection confidence for BGAs and FCBGAs.

The four chief drawbacks of area array packages are as follows:

- Lack of direct visual inspection capability.
- Lack of ability to rework individual solder joints.
- Requirement of multilayer PCB for effective interconnected routing between the chip and the PCB.
- Reduction in thermal cycling resistance due to use of rigid balls.

FCBGAs that are commonly offered for high-performance field programmable gate arrays (FPGAs) have other drawbacks because the die may not be fully engulfed by molding compound materials. During the assembly processes, exposure of non-hermetic FCBGA to cleaning solvent/chemicals or excessive moisture could pose serious package reliability concerns. In one case, small vents were deliberately designed between the heat spreader (lid) and the organic substrate to allow for ease of outgassing and moisture evaporation. The vents, however, became a reliability issue. Cleaning solvents and other corrosive chemicals seeped through these vents, and attacked the organic materials and components inside the FCBGA.

Extensive work was carried out by the author and industry to address the reliability of the previous generations of conventional wire-bonded plastic ball grid array (PBGA) and flip-chip BGA (FPBGA) assemblies [6-22]. Previous work included process optimization, assembly reliability characterization, the use of inspection tools, e.g., X-ray and optical microscopy, and failure analyses to determine quality control parameters and to detect induced and progressive damages with increasing environmental exposures mostly under thermal cycling conditions. The more recent paper was presented on the behavior of System-in-Package (SiP) subjected to thermal cycling and provided failure analyses [23]. Reference 24 addresses the assembly challenges and reliability of newer generation of PBGAs—the current and near future area-array packaging technologies from high I/Os to low pitch packaging technologies. The key results are discussed in Sections 2-5 of this guideline.

1.3 DSBGA PACKAGING TECHNOLOGIES

Key advantages and disadvantages of DSBGAs compared to bare die are listed in Table 1. DSBGAs combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices.

Table 1-1. Pros and cons of die size ball grid array (DSBGA), a.k.a., chip scale package (CSP) and more nomenclatures.

PROS	CONS
Near chip size	Moisture sensitivity
Widely used	Thermal management • Limits package to low I/Os
Testability for known good die (KGD)	Electrical performance
Ease of package handling	Routability • Microvia needed for high I/Os • Pitch limited to use standard PWB
Robust assembly process Only for an area-array version	Reliability is poor in most cases
Accommodates die shrinking or expanding	Underfill required in most cases to improve reliability.
Standards	Array version • Inspectability • Reworkability of individual balls
Infrastructure	
Rework/package as whole	

The advantages offered include smaller size (reduced footprint and thickness), lesser weight, a relatively easier assembly process, lower overall production costs, and improvement in electrical performance. They are also tolerant of die size changes, since a reduction in die size can still be accommodated by the interposer design (fan out) without changing the footprint. DSBGAs have already made a wide appearance in commercial industry because of their advantages, and now, even their three-dimensional (3D) packages are being widely implemented. Unlike conventional PBGA technologies at typically 0.8–1.27 mm pitch, DSBGAs use lower pitches (e.g., currently, 0.8 to 0.3 mm) and hence, will have smaller sizes and their own challenges.

Sections 4-5 present assembly challenges and thermal cycle reliability for die size BGA− CVBGA with 360 balls. It also presents test matrix design, package daisy-chain patterns, detailed design of

PCB, test vehicle design, and detailed information with representative images of various fine pitch area array package and die styles. It also provides examples of assembly of mixed DSBGAs using daisy-chained device including underfilling. The thermal cycle test data in Weibull plots for cycles-to-failures were also presented in Section 5.

1.4 GUIDELINE LIMITATIONS

This guideline addresses COTS BGA/DSBGA packages, quality, and reliability behavior at the assembly level; it does not cover device aspects. Device technologies and assurance methodologies are also of paramount importance and are being addressed by other authors [25]. As semiconductor scaling continues, manufacturing large, defect-free integrated circuits becomes increasingly difficult with added further degradation during screening and use. Reconfigurability of FPGAs enables opportunity for fault tolerance development first by detecting faults, and then by implementing mitigation approaches for the faults.

Device degradation and faults have many mechanisms, including a few shown in the following:

- Degradation due to a hot carrier induced (HCI) effect that leads to a buildup of trapped charges in the gate-channel interface region.
- Degradation due to negative biased temperature instability (NBTI), which presents similarly to buildup of trapped charges.
- Degradation due to electromigration (EM) mechanisms, in which metal ions migrate over time, leading to voids and deposits in interconnections, eventually causing faults due to the creation of open and short circuits.
- Degradation due to time-dependent dielectric breakdown (TDDB), which affects the gates of the transistor, causing an increase in the leakage current and eventually a short circuit.
- Faults due to manufacturing defects can be exhibited in circuit nodes as stuck, and switch too slowly to meet the timing specification, or cause short or open circuit.
- Faults due to radiation exposures, including single event upsets (SEUs) and single event transients (SETs). The most commonly considered failure mode is the flipping of a static random access memory (SRAM) cell in the configuration memory.

In general, COTS Electrical, Electronic, and Electromechanical (EEE) parts including BGAs and specifically DSBGAs do not have space heritage. If they have been used in the past, they are already obsolete or have been replaced with new generation because of their short life span in industry.. This poses significant challenges on establishing traceability and heritage applicability as well as establishing long-term quality and reliability requirement for mission.

Understanding the deficiencies of COTS EEE and the successful implementation of COTS packaging technologies at assembly level that meet Mission Environment Applications and Lifetime (MEAL) requirements is critical and is addressed in this document. The guideline categorizes BGA packaging technologies from their application robustness, e.g., BGAs or DSBGAs, as well as generically categorizes a number of NASA's MEALs, e.g., short benign or long extreme, with the risk posture of a mission in order to narrow recommendations on use of COTS BGAs/DSBGs for

numerous mission scenarios. Detailed recommendations are presented with technical rationale. Three key areas addressed in the guideline are:

1. Test matrix and board level thermal cycle reliability evaluation test data for BGAs and FCBGAs assemblies. Both a relatively benign thermal cycle (–55°C /100°C) and severe thermal shock (–65°C /150°C) test were performed to compare the results and applicability of acceleration. Note that that this temperature shock cycle range is harsh and was used to determine the short effect of 150°C exposure since this temperature was used by a number researchers to determine by isothermal aging the integrity of ENEPIG surface finish. In addition, since ENEPIG finish was used as a variable, it provided high-reliability industries with additional information on microstructural changes at interfaces.
2. Test matrix and board level thermal cycle reliability evaluation test data for assemblies of die size BGAs. Only one thermal cycle condition (–40°C /125°C) is presented since there were numerous process variables considered in the test matrix and this was a common cycling performed by an industry partner.
3. Detailed recommendations of BGAs/DSBGAs for NASA missions with the consideration of MEAL requirements. Lessons learned from items #1 and #2 are covered, as well as a literature search and experiences from spaceflight implementation of advanced electronics packaging technologies and COTS BGAs. Specific recommendations are given for low risk infusion NASA missions with the consideration of MEAL requirements.

2 BGA/FCBGA ASSEMBLIES UNDER THERMAL CYCLING

2.1 TEST MATRIX

To determine assembly reliability of BGAs and FCBGAs packaging technologies, packages with a daisy chain patterns are required. The PCB was designed to match BGA daisy chain patterns. Not all package styles from a manufacturer come in daisy-chain form; generally, manufacturers only select representative packages and offer them as a daisy chain, so the choice of packages for evaluation is generally limited. Only one package chosen did have a daisy chain pattern. The daisy chain patterns on PCBs were designed to complement BGA patterns, forming a complete loop after assembly. The resistive loops were monitored during thermal cycling to allow detection of open loops due to solder joint opens of BGAs onto a PCB.

A complex PCB was designed to accommodate the various BGA/DSBGA styles with the consideration of processing challenges and reliability evaluation aspects. Figure 2-1 shows the board design, with daisy chain pattern, and how traces are routed to the edge of the board for daisy chain monitoring. A design of experiment (DOE) technique is used to cover various aspects of packaging types and pitches, processing variables, and packaging assembly reliability.

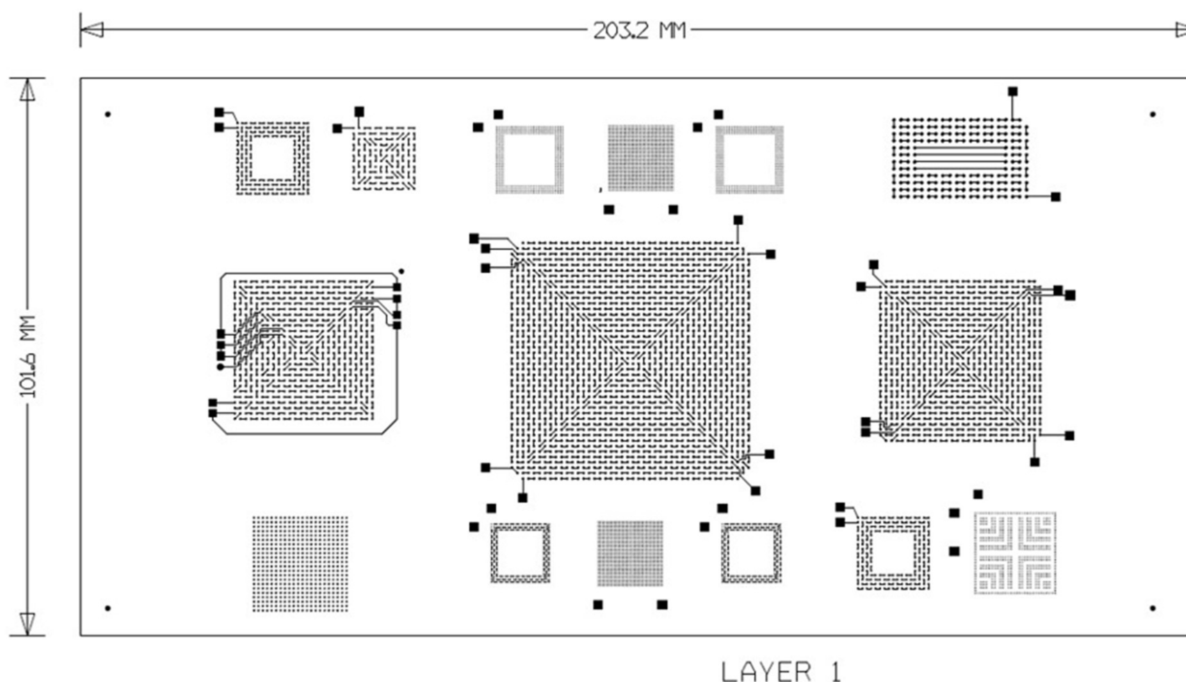

Figure 2-1. Test vehicle design showing daisy chain patterns for package from 1924 I/O flip-chip BGA (FCPBA) package with a 1 mm pitch to 1600 I/O wafer level package (WLP) with 0.3 mm pitch.

2.2 PACKAGE STYLES

The following packages with package type, size, pitch, and number of balls were designed in preparation for assembly and subsequent reliability testing. The following list shows the BGA/FCBGA packaging parameters that are considered as part of a larger DOE implementation.

- Four daisy chain COTS BGA packages with 1 mm pitch from four suppliers were selected for evaluation. Three packages built with SnPb solder balls and one with Pb-free balls. The FCBGA1924 with 1.0 mm pitch and 45 mm^2 body size design at the center of the board.
- Two 1 mm pitch BGAs on the two sides of the FCBGA1924 package. On the right side is a PBGA891 with 3 mm^2 body size.
- BGA676 with 27 mm^2 body size was designed in a previous test vehicle and is used here as the baseline for comparison. The fourth PBGA has Pb-free SAC 305 (Sn96.5 Ag3 Cu0.5) solder balls and is categorized as thin core BGA (CTBGA) with 144 balls and 13 mm^2 body size.
- Three BGAs with 0.8 mm pitch, two with daisy chain and one functional part with no daisy chain patterns. Chip array BGA with 208 I/O and CTBA208 with two different packaging technologies had the same 15mm^2 body size. CABGA has SnPb solder balls whereas CTBGA has Pb-free SAC305 solder balls. Very fine pitch flip-chip ball grid array (FCV-BGA) with 484 balls had no daisy chain pattern and had SnPb solder balls. This package is located at the bottom left corner and designed as such that to be able to cut the part for evaluation at cycle intervals.
- A 3D stack daisy chain BGA package with 1.27 mm pitch, 29 mm by 19 mm body size, and 191 high-lead solder balls, which becomes sensitive to maximum reflow temperature. This stack BGA package is replacing the leaded TSOP version to meet the demand in memory increases. Figure 2-2 shows photomicrograph images of this package showing the package and ball interconnections. The quality of these joints is considered to be acceptable. All packages were inspected, cleaned, and baked before assembly.

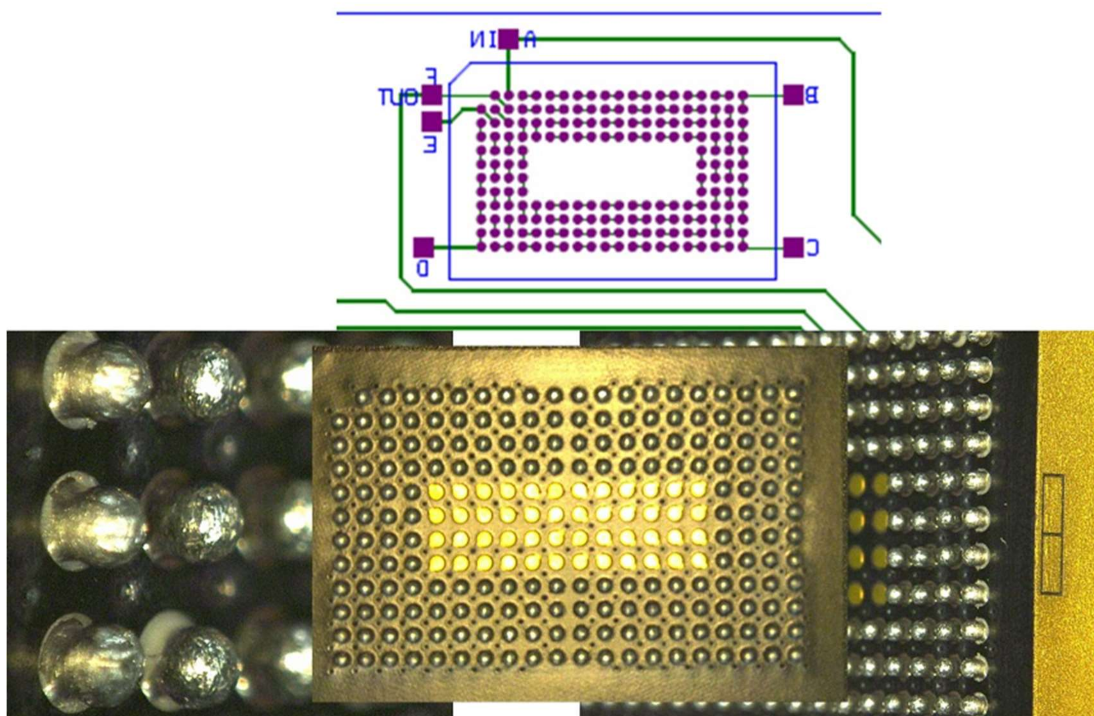

Figure 2-2. Daisy chain pattern (top) and photomicrographs (bottom) showing various aspects of package and solder attachment configuration for the 3D stack package.

2.3 PCB DESIGN AND SURFACE FINISH

PCBs were made from high glass-transition temperature (Tg) FR-4 ROHS materials with 0.093-inch thickness and double-sided. They had an ENEPIG (electroless Nickel electroless palladium and immersion gold with thickness of Ni = 118-236 µin, Pd = 4 µin minimum, Au = 1.2µin minimum. Other parameters were board size of 4" x 8", four layers, 416 copper-fill vias at 0.150 mm, and 5540 vias at 0.100 mm, at layer 1-2. Figure 2-3 shows the enlarged PCB pads for a number of package configurations; those with via-in-pad (ViP), i.e., daisy chain link between layer 1-2, are identified. Daisy chain patterns were designed at the surface of PCB for a larger pitch package including FCBGA1924 and 3D stack with 191 high-lead balls. However, daisy chain patterns were moved between layer one and two (trace in layer two) for DSBGAs.

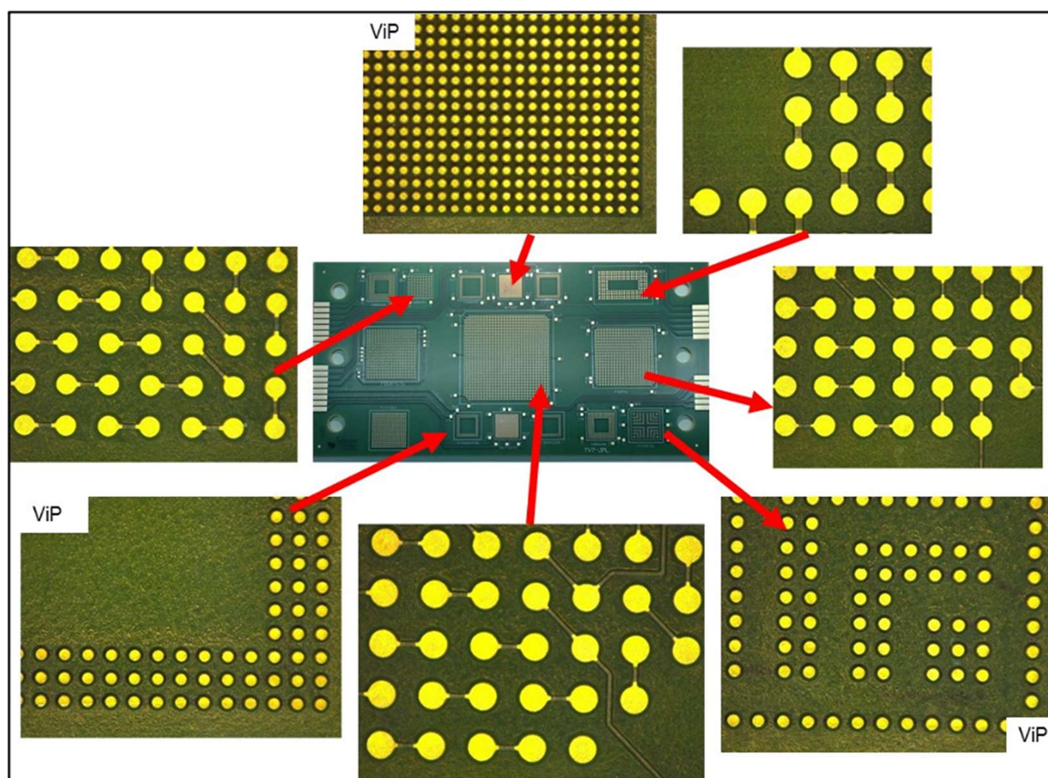

Figure 2-3. Printed circuit board (PCB) with representative enlarged daisy chain patterns showing standard daisy chain links on the surface (layer 1) for larger pitches and those with via-in-pad (ViP) between layer one and two for finer pitch patterns.

2.4 LIMITATION OF HASL FINISH FOR BGA AND ENEPIG FOR DSBGA

Figure 2-4 shows a section of the PCB that compares the images of daisy-chained pad patterns for ENEPIG and HASL. The baseline for the pitch of 1.00 mm is also included. It illustrates irregularity in HASL for DSBGA and acceptability of ENEPIG finish. The HASL shows solder shorts covering four pads. Even the solder dome formation is non-uniform. The ENEPIG finish, however, shows excellent consistency for a 0.3 mm pitch and higher. Thus, the ENEPIG is a clear winner. For a 0.4 mm pitch, the HASL finish is more consistent even though solder dome formation is still a common feature.

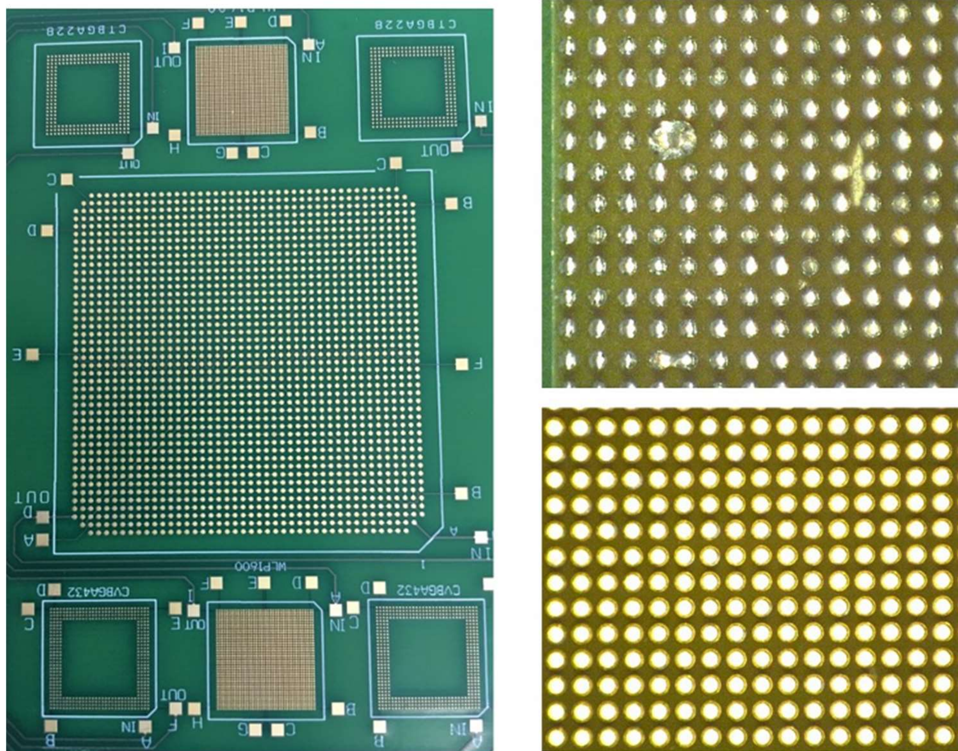

Figure 2-4. The images of HASL (left) and ENEPIG (right) PCB finishes. The HASL finish is unacceptable for WLP1600 with 0.3 mm pitch, whereas ENEPIG is acceptable.

2.5 ASSEMBLY PARAMETERS FOR A MIXED BGA & DSBGA

Optimization of the assembly process should always be considered for a mixed BGA and DSBGA build. The process steps presented below were modified for optimization during implementation based on daisy chain continuity checks and X-ray evaluation. These steps were modified as needed in order to optimize processes based on daisy chain and X-ray evaluations after each assembly.

- Perform package and PCB inspection for workmanship.
- Bake out packages and PCBs after cleaning.
- Start with using a standard 4 mil-thick stencil for paste printing of the whole board. However, a mini stencil with 4 mil thickness may be required for paste printing locally when it is required to accommodate a specific package assembly, including the large size FCBGA1924. Rework station equipment may also be used for local heating and assembly.
- Start with type IV tin-lead solder paste for the all-package assembly. Use finer solid solder paste, i.e., type V, to accommodate finer pitch packages in order to optimize assembly of all packages.
- Measure solder paste volumes at the four corners and at the center for these assemblies to document actual paste-print volume, distribution, and solder-paste release efficiency. Use these data to optimize assembly processes.

- Use a vapor-phase reflow machine to assemble all packages, including the FCBGA1924. When it is required as part of the DOE design, assemble PBGA and FCBGA with a 1 mm pitch using a rework station.
- Add corner staking or spot bonding to strengthen the larger packages, enabling increasing resistance to mechanical loading as well as to determine the effects of bonding on failure behavior under a thermal-cycling condition.

Manufacturing robustness of various package configurations were determined by daisy chain continuity checks followed by optical and X-ray inspection. Then, they were subjected to thermal cycling for reliability and failure mechanism characterizations.

2.6 OPTICAL INSPECTION AFTER ASSEMBLY

For BGA/DSBGA package assembly, X-ray evaluation is needed to determine shorts and possibly, on rare occasions, for opens. Visual inspection with optical microscopy is of limited use since it is difficult to inspect peripheral ball interconnections and impossible to inspect hidden balls under the package, except with special tools and set up. For the test vehicle with daisy chain package configuration, verifications were performed: (1) through daisy chain resistance continuity checking, (2) through X-ray quality detection for shorts and in on rare occasions for opens, and (3) through visual inspection, specifically peripheral solder joints for the 3D stack assemblies.

Figure 2-5 shows an optical image covering three different assemblies of PBGA package styles with different sizes and pitches. The I/Os varied from 191 to 896 and pitches from 0.8 to 1.27 mm. As apparent, the 3D package is taller than the other PBGA package. The 3D packages become more susceptible to overheating due to the infrared (IR) preheating zone of the vapor phase machine used for reflowing solder paste. Process optimization also took this aspect of assembly into consideration. Package blistering due to overheating at IR is considered one potential defect that must be avoided, especially knowing more susceptibility of this package to moisture absorption. In addition, the solder for the 3D package was high lead solder that, contrary to eutectic tin-lead solder, did not melt during a tin-lead solder reflow process. Figure 2-6 shows the solder joint quality of the 3D stack after assembly. It clearly shows good peripheral solder joints and acceptable fillet formation. Two solid solders are present, one with original un-melted solder balls attached to package and the other with melted solder paste forming solid solder disks attached to PCB.

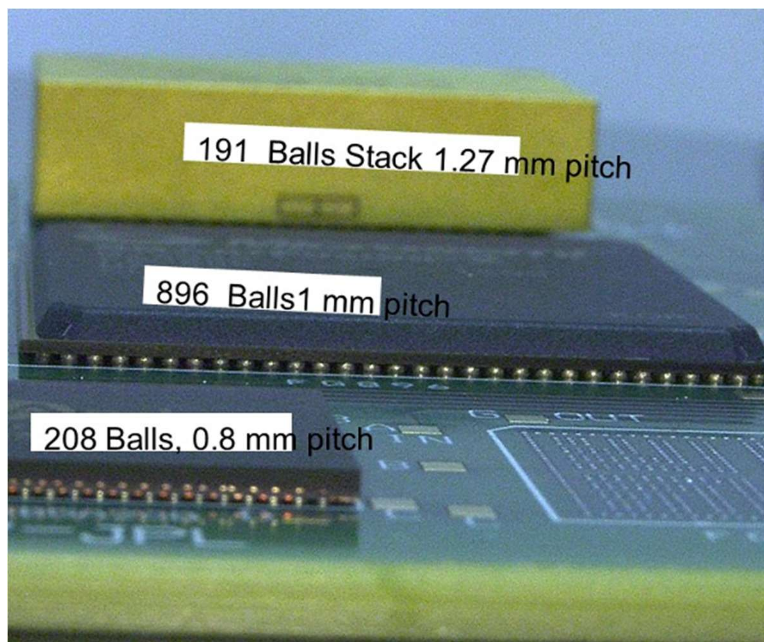

Figure 2-5. The close-up image shows three PBGA assemblies covering I/Os of 208 and 896 I/Os, and a 3D stack with 191 I/Os. Pitches were 0.8, 1.0, and 1.27 mm, respectively.

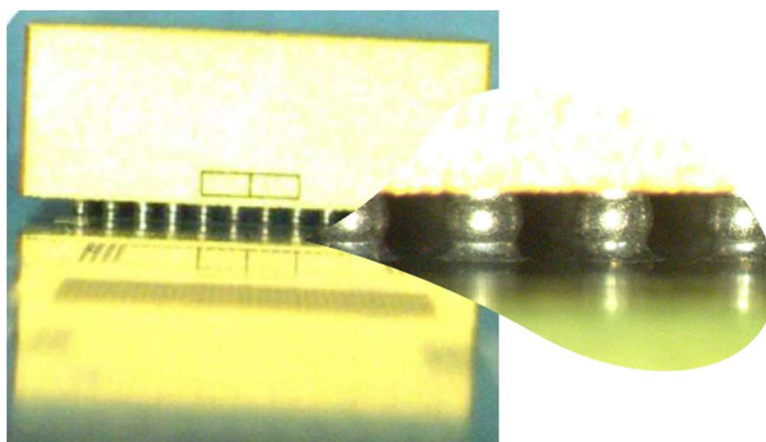

Figure 2-6. The image shows the overall 3D stack package assembly with an enlarged image showing more detail of the solder joint interconnections. Two solid solders, one with original un-melted solder balls attached to package and the other with melted solder paste forming solid solder disks attached to PCB.

2.7 BGA X-RAY CHARACTERIZATION AFTER ASSEMBLY

The 2D real time X-ray transmission system, direct or with oblique-angle views, was used for BGA assembly inspection. An overall X-ray photomicrograph for the 3D stack assembly showed features of the package as a peripheral area array as well as assembly characteristics showing no signs of shorts or existence of solder balls. Figure 2-7 shows X-ray photomicrographs of the 3D stack package assembly taken at high magnifications with an oblique view showing features of the corner balls. The X-ray shows mostly dark circular patterns with a lighter section expanding to the darker area. The lighter areas appear to have even lighter spots that possibly represent a number of small

voids at the PCB solder joints. The dark area represents the original high-lead solder balls and the lighter areas are the solder disk formed from eutectic tin-lead solder paste during assembly. Even at this high magnification, there were no signs of shorts or solder balls.

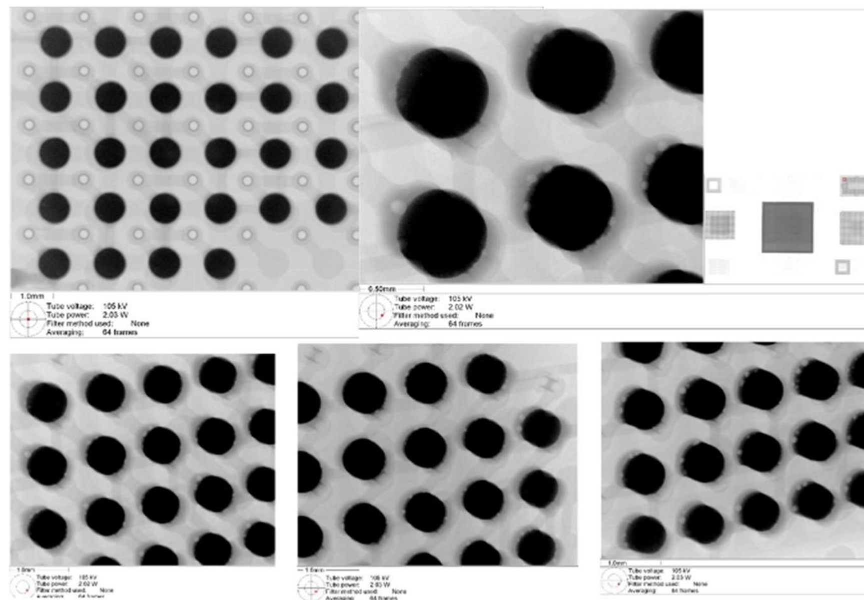

Figure 2-7. Representative X-ray photomicrographs of the 3D stack package assembly at various oblique angle views.

The X-ray images of FCBGA1924 are shown in Figure 2-8. The image shows that this package is fully populated and shows a region of darker area at the center—the flip-chip die area. X-ray images at higher magnifications are also included in the Figure. The X-ray image that shows the corner of the die reveals a large number of small circular dark dots that are representative of the flip-chip balls within the die. The balls are much smaller than the package balls and with much higher density.

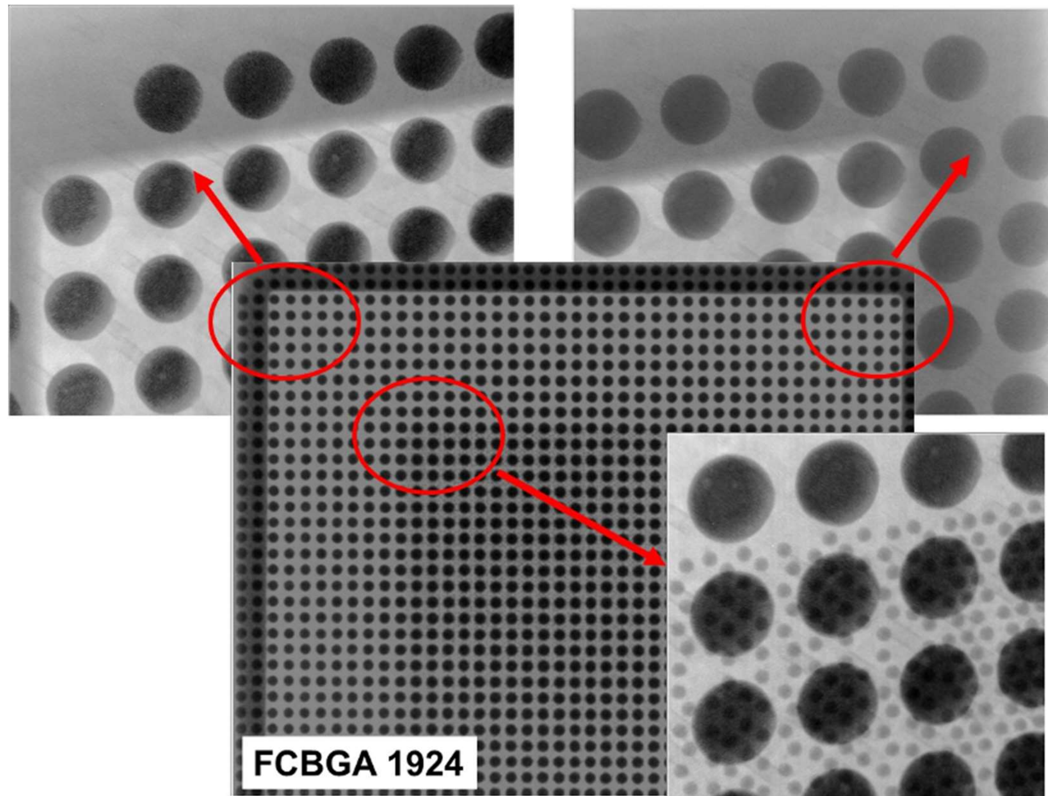

Figure 2-8. X-rays for the FCBGA1924 showing images of corner balls (top left and right) as well as an X-ray image for the corner die showing solder balls for the flip-chip die.

Figure 2-9 shows X-ray images of wire-bond PBGA896 and PBGA676. The dark center area is the die section has no smaller solder balls, as was the case for the FCBGA1924, since the two packages have internal wire-bonded die. X-ray images of the corner solder balls are also shown at higher magnifications. These also show no signs of solder balls, shorts, or opens. Note the die size relative to package size. The ratio is much larger for PBGA676 relative to PBGA896 that should be considered in cycles to failure. The larger ratio package is more susceptible to earlier failure for full array BGAs.

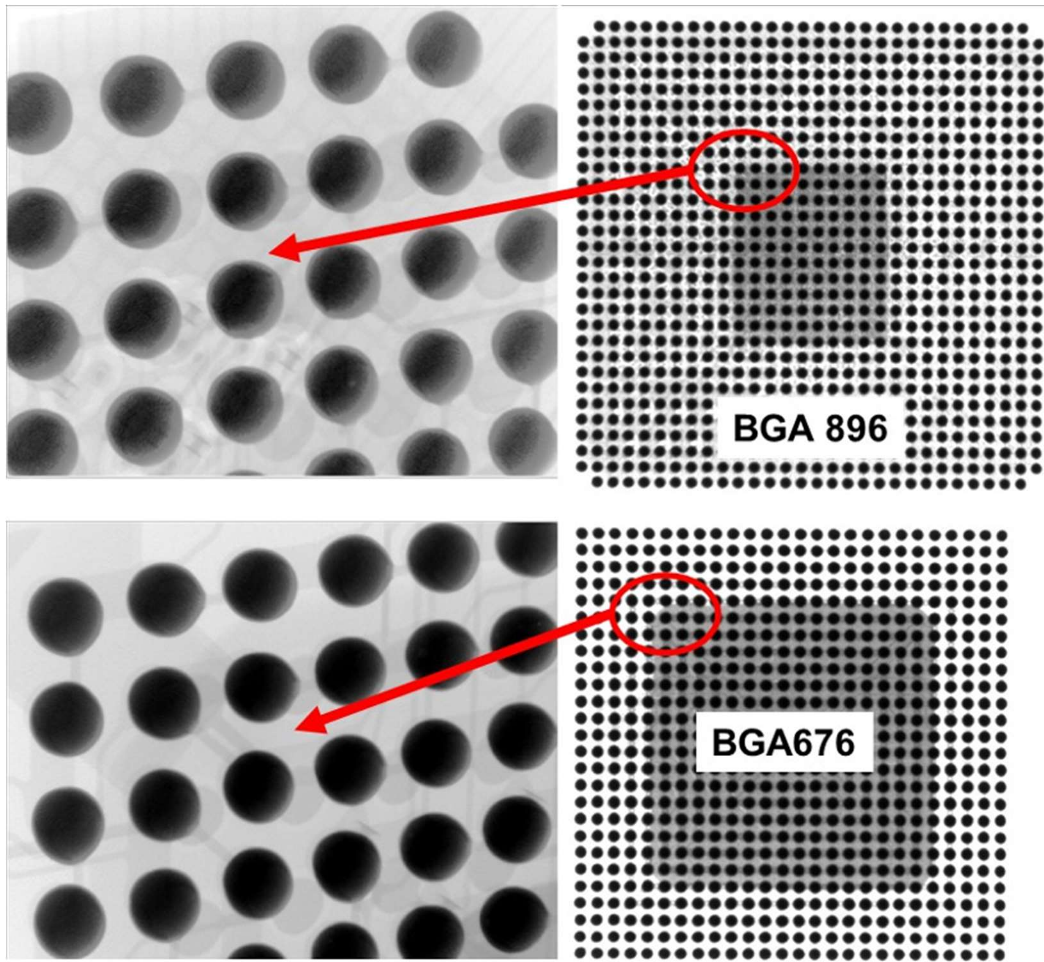

Figure 2-9. Overall X-ray images for the PBGA896 and PBGA676, which also include images of corner balls at a higher magnification.

Figure 2-10 shows X-ray of PBGA208 with peripheral array balls, but two solder metallurgy: SAC and tin-lead solders. X-ray images of corner solder balls at higher magnifications are also included. There are no signs of solder balls, shorts, and opens. Also, the X-ray images do not reveal any features suggesting that the solder balls for the two packages have different compositions.

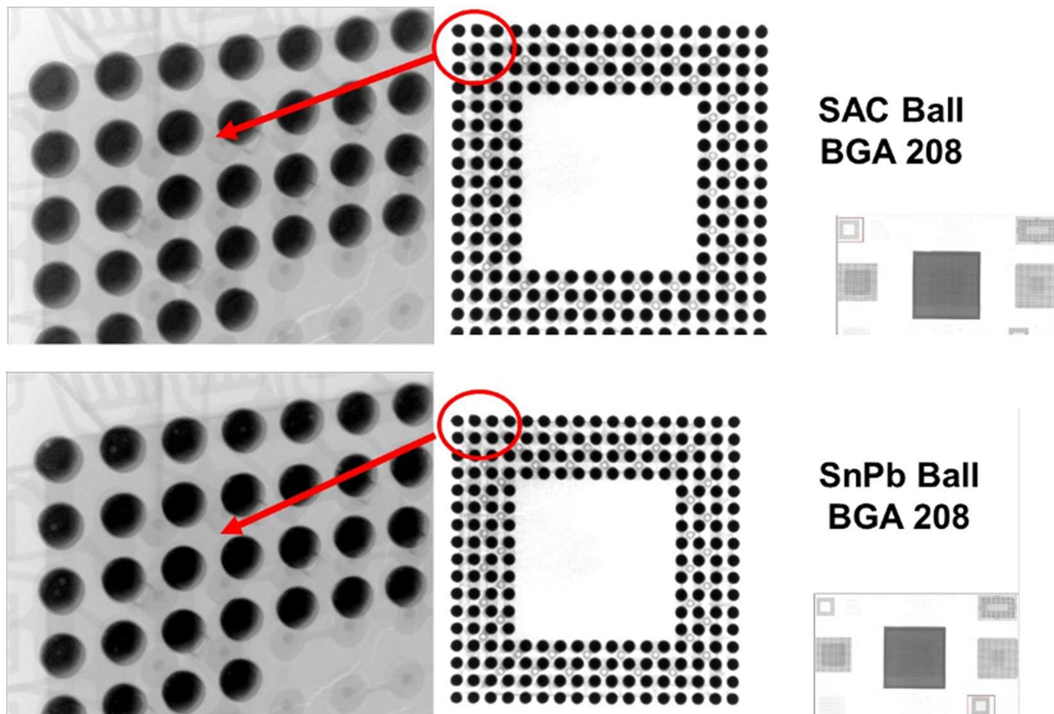

Figure 2-10. Overall X-ray images for the PBG208 with SAC solder balls (top) and tin-lead solder balls (bottom). The arrows point to X-ray images of the corner balls at a higher magnification.

3 BGA THERMAL CYCLES (–55/100°C OR –65/150°C)

3.1 BGA THERMAL CYCLES (–55°C /100°C)

Five test vehicles, one with a double-sided assembly, each with six packages [3D stack, PBGA676, PBGA896, FCBGA1924 and two PBGA208 (SAC and tin-lead solder balls)], were subjected to thermal cycling for reliability evaluation. Thermal cycle testing was conducted in the range of –55°C to +100°C as specified in the IPC 9701, 10-15 minutes dwells at 100°C and –55°C with 3-5 °C/min ramp rate that also met the dwells and the ramp requirement of requirement of being less than or equal to 20°C/min.

After 200 thermal cycles (–55°C to +100°C), there was no resistance open for the 3D stack nor the other five PBGA packages. The 3D and PBGAs were also inspected by optical microscopy at 100 and 200 thermal cycles. There were no apparent failures noticed for PBGA and clearly for peripheral array of 3D stack package assemblies. Figure 3-1 shows optical photomicrographs of a single-sided 3D stack package assembly (SN001) after 200 thermal cycles. It shows no apparent solder micro-cracking. Furthermore, visual inspection via optical microscopy revealed a minimal change in microstructural features of the peripheral solder joints of 3D stack assemblies. The peripheral solder joins of 3D stack could be partially inspected, partially blocked by the package vicinity. It was concluded that damages were minimal due to 200 thermal cycles (–55°C to +100°C).

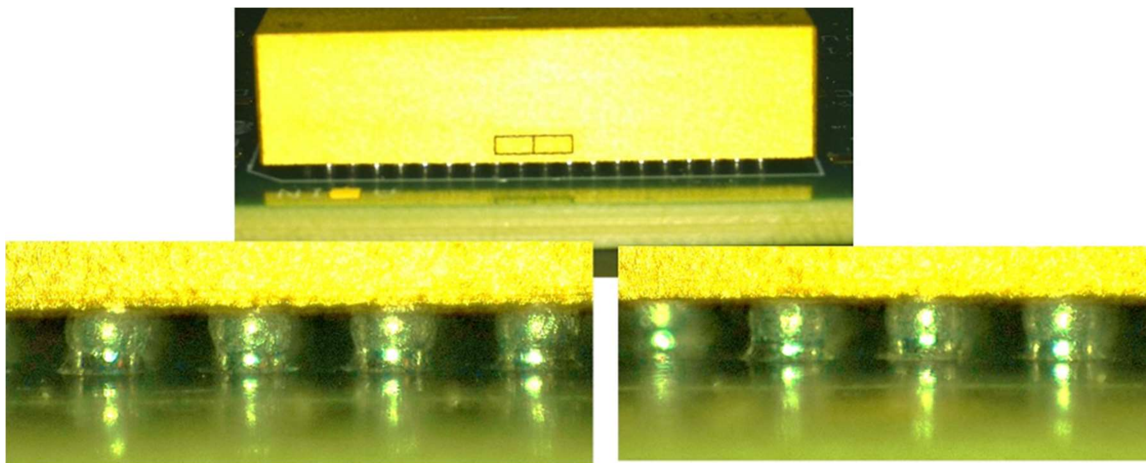

Figure 3-1. Optical photomicrographs of single-sided 3D stack package assembly after 200 thermal cycles (–55°C to +100°C).

Figure 3-2 shows the double-sided 3D stack assembly (SN005) after 200 thermal cycles. This assembly had corner staking to determine the effect of double-sided assembly and also possibly the negative effect of adhesive bonding. There are no significant effects of the two parameters at this stage of thermal cycling. Results may differ at higher thermal cycles.

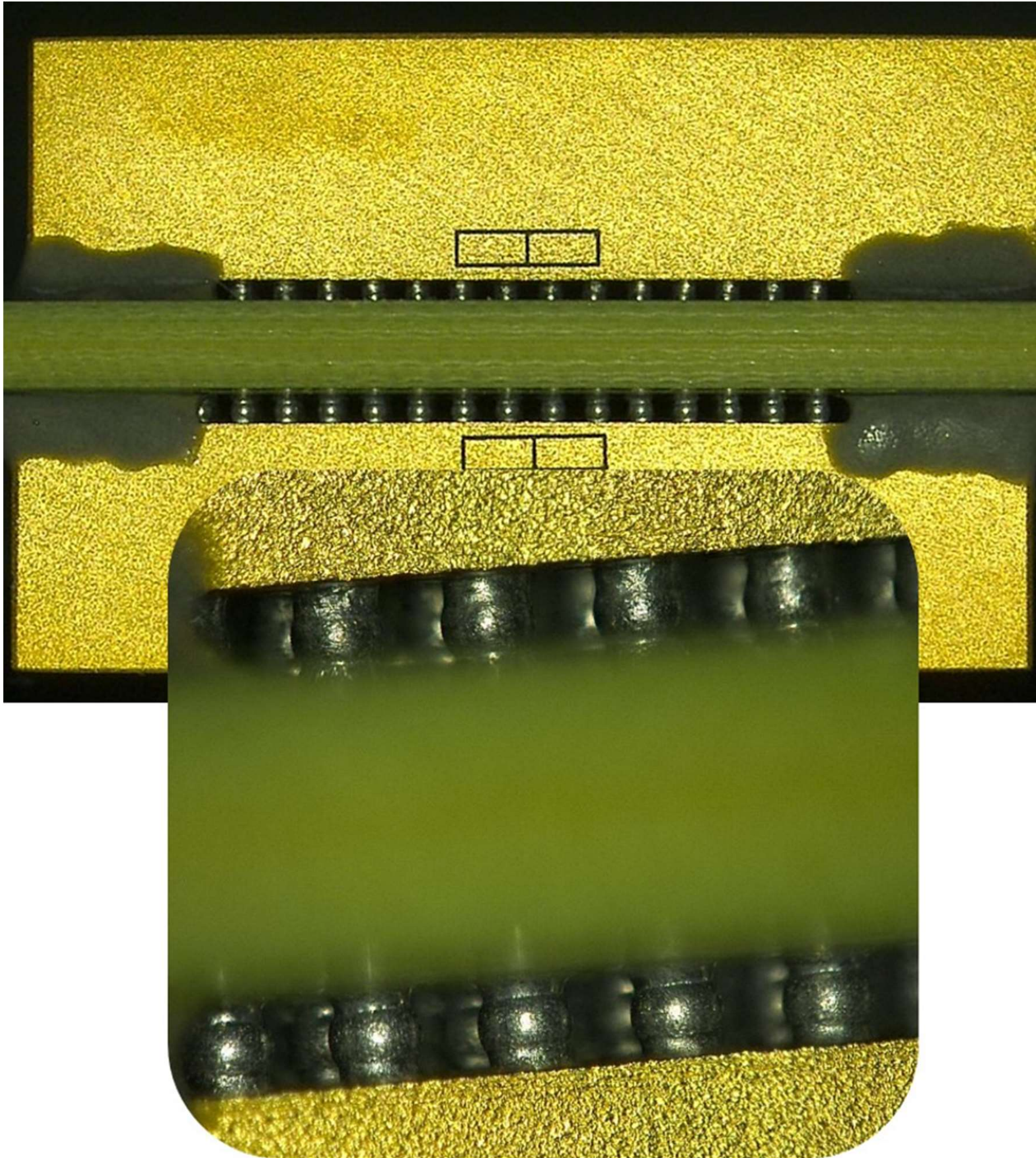

Figure 3-2. Optical photomicrographs of a single-sided 3D stack package assembly after 200 thermal cycles (–55°C to +100°C).

Figure 3-3 compares optical photomicrographs of PBGA208 with SAC and tin-lead solder balls assemblies after 200 thermal cycles (–55°C to +100°C). Optically, the only difference is the increased graininess of SAC solder balls. There are otherwise no apparent differences between the solder ball compositions. Both showed no daisy chain resistance changes. Thermal cycles at higher levels could reveal the effect of using SAC vs. tin-lead. Figure 3-4 shows the condition of a number solder joints for a FCBGA1924 assembly after 200 thermal cycles. There is no apparent separation, which is also consistent with having no daisy chain opens.

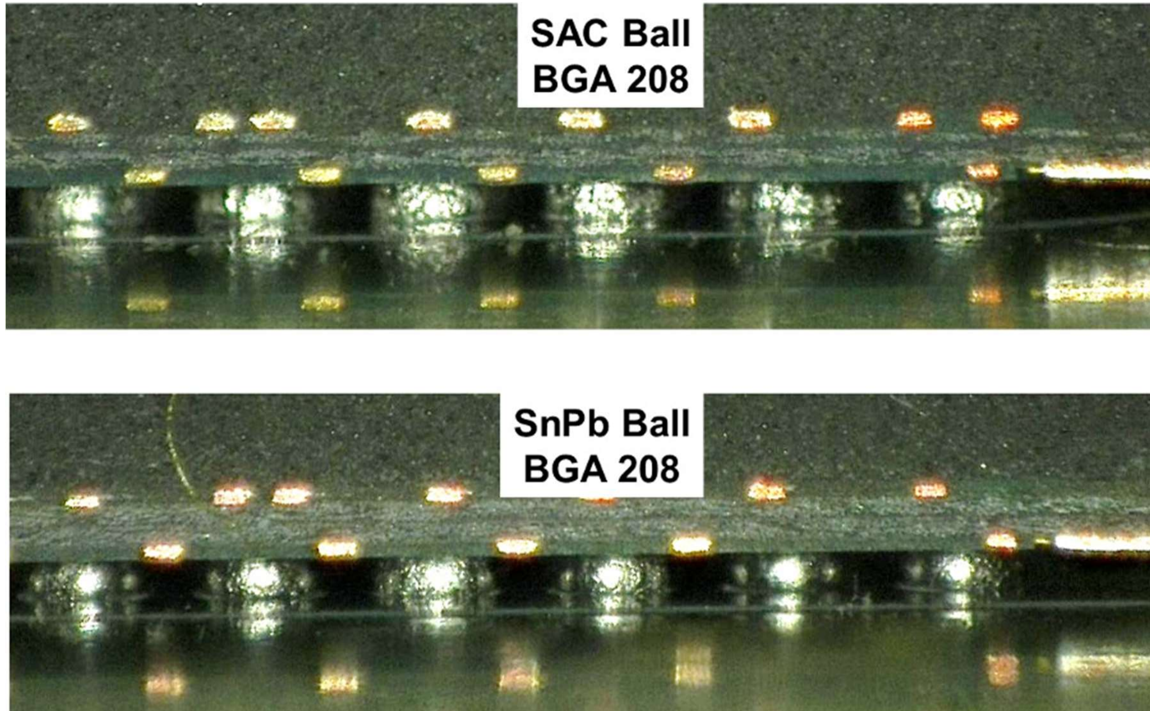

Figure 3-3. Optical photomicrographs of PBGA 208 with SAC (top) or tin-lead (bottom) solder balls after 200 thermal cycles (–55°C to +100°C).

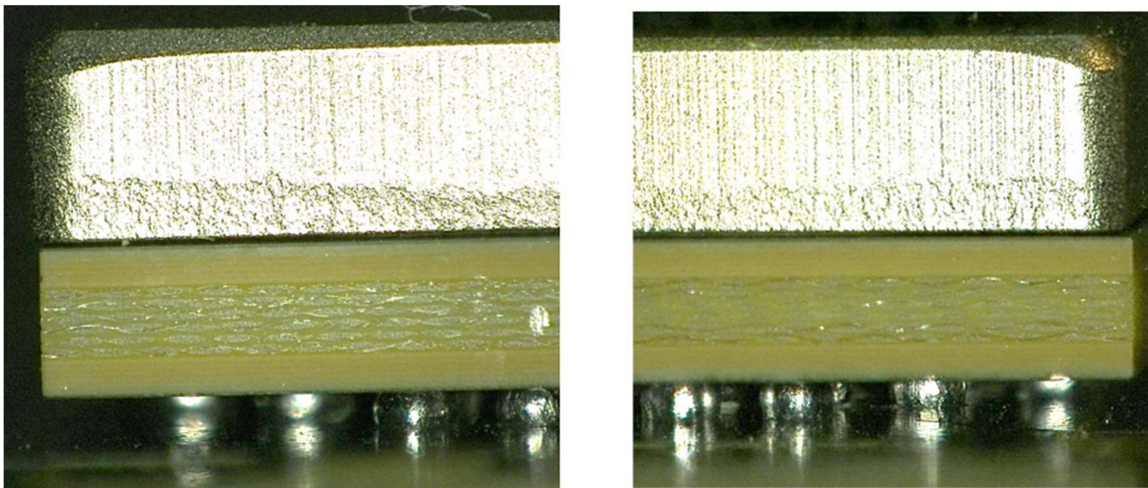

Figure 3-4. Optical photomicrographs of FCBGA1924 after 200 thermal cycles (–55°C to +100°C).

3.2 BGA THERMAL SHOCK CYCLE (–65°C /150°C)

Two test vehicles (TVs), one with ENEPIG and the other with HASL PCB finish, were subjected to a higher temperature cycling range to possibly induce failures and to determine the effect of an elevated temperature on microstructural metallurgy at interfaces. The two TVs were subjected to thermal shock cycles in the range of – 65°C to 150°C. Contrary to thermal cycle condition, which was performed in one chamber, the thermal shock (TS) cycle used two chambers and the two TVs

were shuttled between the hot and cold chambers. After 200 TS cycles, no failures were detected by the daisy chain resistance measurement for the 3D stack, PBGA676, PBGA896, and FCBGA1924. Numerous failure analyses including microstructural evaluations were performed to characterize behavior of solder and interface after 200 TS cycles. Analysis results are presented for the FCBGA1924 with ENEPIG or HASL PCB finish.

Figure 3-5 illustrates representative images of cross-sectional photomicrographs for FCBGA1924 showing microstructural characteristics of solder joints for PCB with HASL finish. Except for minor voids, there were no apparent other anomalies. Images taken at higher magnifications show more detailed information on the intermetallic characteristic at the package/PCB interfaces (see Figure 3-6). To verify microstructural observation with no solder cracking, half of the cross-sectional specimen was subjected to dye-and-pry to determine solder/pad interface characterizations in a wider scale— more than 900 solder joint interconnections.

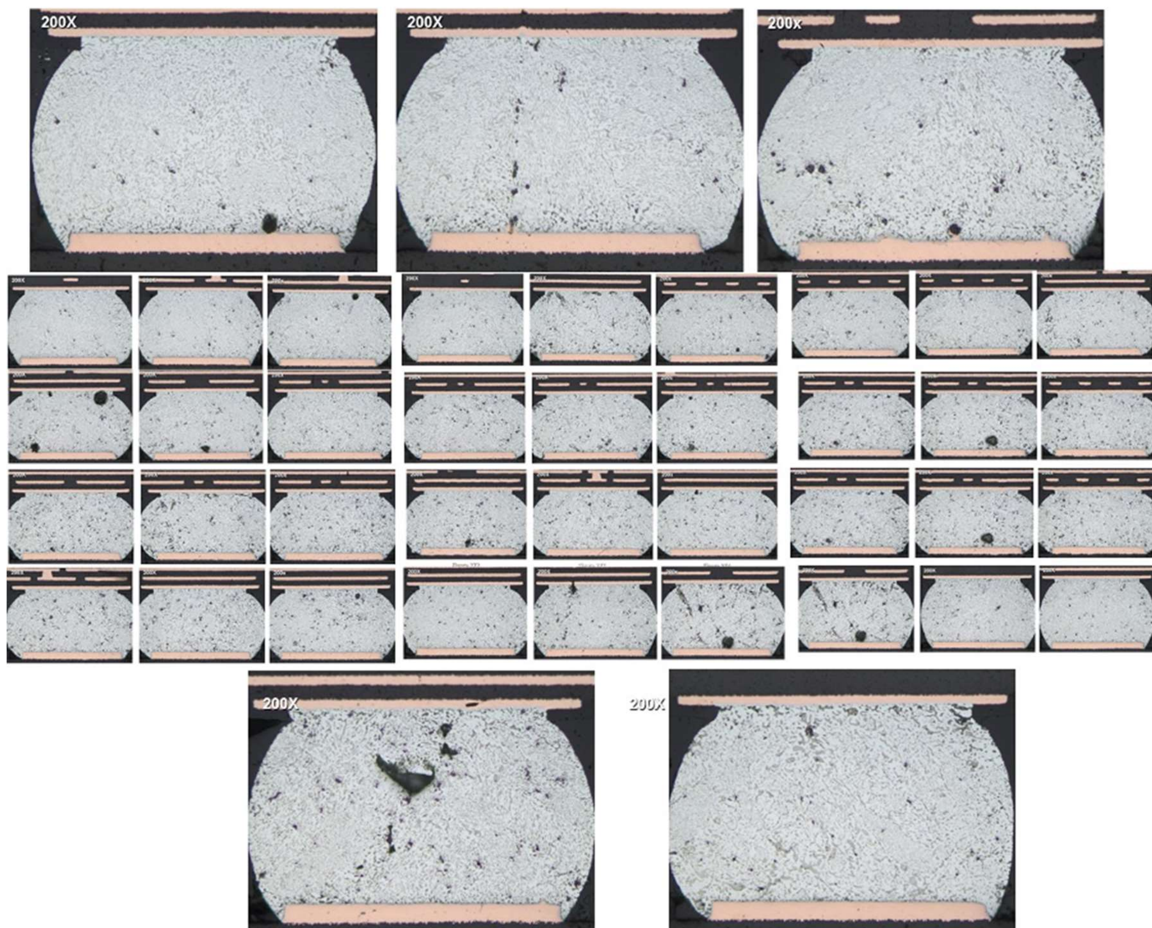

Figure 3-5. Representative cross-sectional images of solder ball and interface HASL (SN12) from top to bottom and from left to right for FCBGA/SN12 after 200 thermal-shock cycles (– 65°C /+150°C).

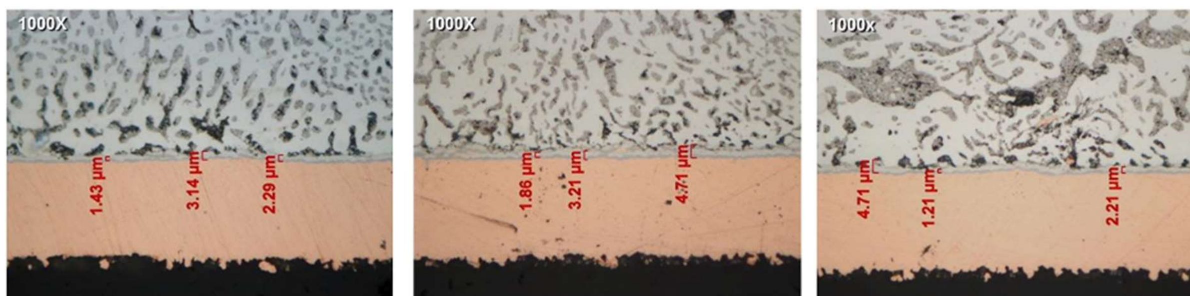

Figure 3-6. Representative HASL IMC at interfaces (SN12) for FCBGA after 200 thermal-shock cycles (– 65°C /+150°C).

Figure 3-7 shows red dye stain on both PCB and BGA pads after prying. There is no evidence of microcracking and separation. All the pads with daisy chain traces intact were separated from the PCB and remained on the balls of the package. This indicates the weakness of the pad bonding to its epoxy under layer. The lack of existence of partial or full dye stain on the board or package also confirms the observation of lack of resistance changes in daisy chain and is in agreement with lack of significant microstructural cracking of cross-sectioned sample after 200 TS cycles.

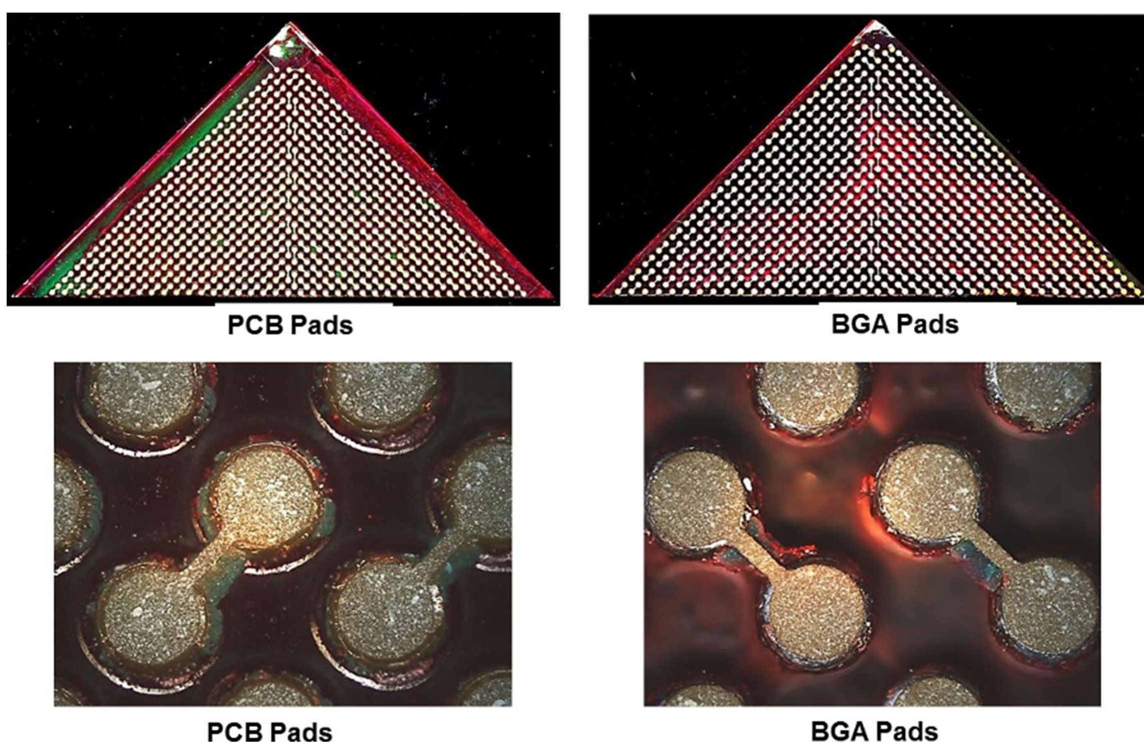

Figure 3-7. Representative dye-and-pry optical images for the FCBGA1924 assembly onto tin-lead HASL PCB surface finish after 200 TS (– 65°C /150°C). Left images are for PCB pads and right images are for BGA pads.

Figure 3-8 shows a SEM image of HASL IMC at higher magnification delineating more detailed information on microstructural characteristics of HASL IMC for FCBA1924 after 200 TS. It also includes elemental distribution of solder and interface performed by energy dispersive X-

ray/spectroscopy (EDX/EDS). Figure 3-9 compares SEM/EDS images for the HASL IMC (bottom) and ENEPIG IMC (top) for FCBGA1924 assemblies after 200 TS (– 65°C /150°C).

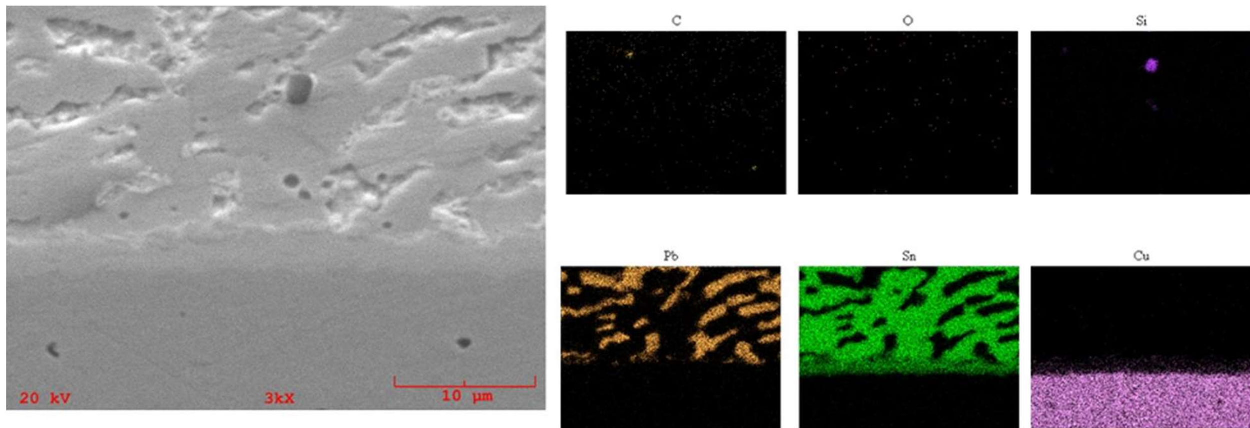

Figure 3-8. SEM/EDS images for the FCBGA1924 assembly onto HASL PCB surface finish after 200 TS (– 65°C /150°C).

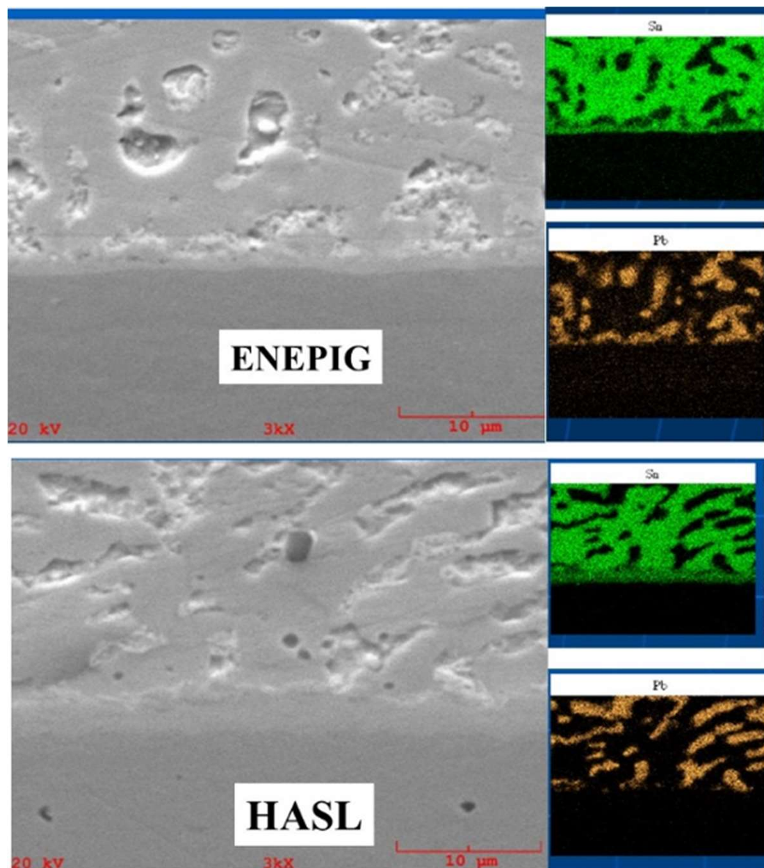

Figure 3-9. SEM/EDS images for the FCBGA assembly onto ENEPIG (top) and tin-lead HASL (bottom) PCB surface finish after 200 TS (– 65°C /150°C).

4 DSBGA ASSSEMBLIES UNDER THERMAL CYCLES

4.1 TEST MATRIX

To determine assembly reliability of DSBGA packages and device technologies, devices with daisy chain patterns are required. Like the BGA test plan, the PCB was designed to match device daisy chain patterns. For this evaluation all packages/devices had dais -chain patterns. This enabled monitoring of solder joint integrity either for manufacturing workmanship (e.g., open) or resistance monitoring during thermal cycling. The assembly resistive loops were monitored during thermal cycling to allow detection of open loops due to solder joint opens of these packages/devices to a PCB.

A complex PCB was designed especially for CP-FC to accommodate the various device styles with consideration of processing challenges and reliability evaluation aspects. The top left image of Figure 4-1, shows the first layer of the board design with a daisy chain pattern, and how traces are routed to the edge of the board for daisy chain monitoring. The top right image shows the second lay of the board design with selected daisy chain patterns implemented through Via-in-Pad (ViP) microvias. The bottom image shows an FR-4 PCB with 0.91-inch thickness ready for assembly. A test matrix covered various aspects of the part types and pitches, processing variables, and packaging assembly reliability. However, the initial test plan could not fully be implemented for reliability evaluation due to numerous assembly challenges.

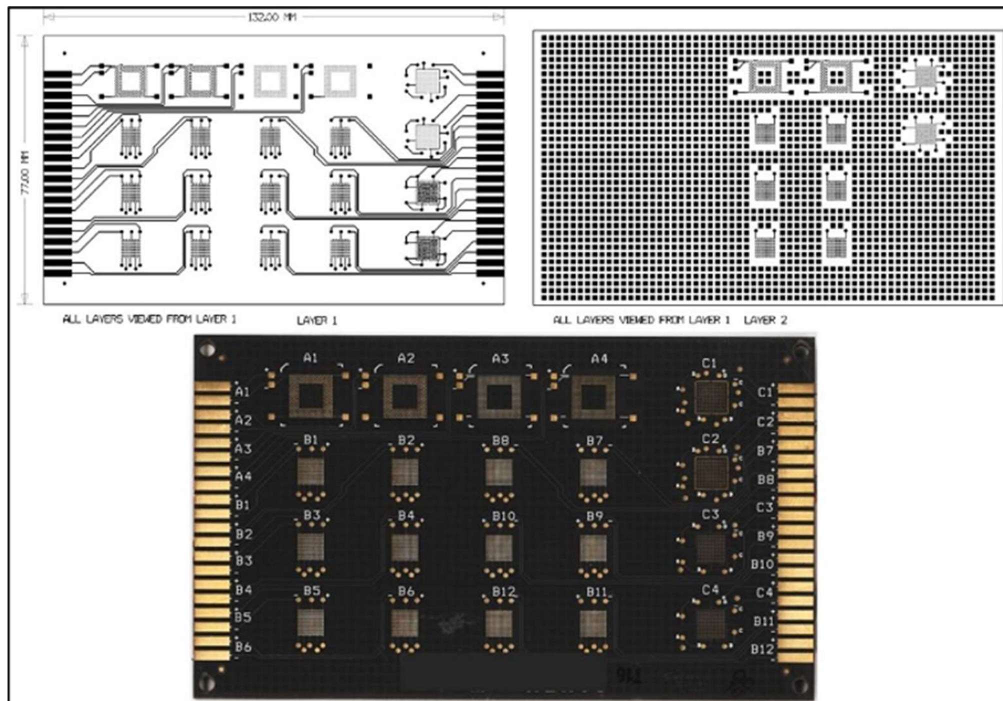

Figure 4-1. Test vehicle design showing daisy chain patterns for package/devices from CVBGA360 I/Os, (top side, four locations), CP-FC 1048 I/Os (right side, four locations), and eWLP (left side, 12 locations).

4.2 PACKAGE STYLES

Figure 4-2 schematically shows the concepts of the three types of devices considered in this evaluation, die-size BGA, Cu-pillar flip-chip die (CP-FC) and Wafer Level Package (WLP). It may be apparent that packaging is designed to accommodate the lagging miniaturization of the printed circuit board (PCB) since such miniaturization adds significant cost to the final product. For this reason, electronic functional chips are transformed by various packaging schemes that enlarge the die features for ease of assembly as well as protecting from environment. BGA to WLP, molded and more recent fan-out configurations, are the purpose of the microelectronics packaging technologies. An interposer is used to accommodate the fine pitch of the chip as well as the next level interconnection, e.g. PCB. For this reason, direct attachment of CP-FP is considered to be challenging. The daisy chain at the PCB level was modified to accommodate PCB trace/pad size limitation with significant hurdles.

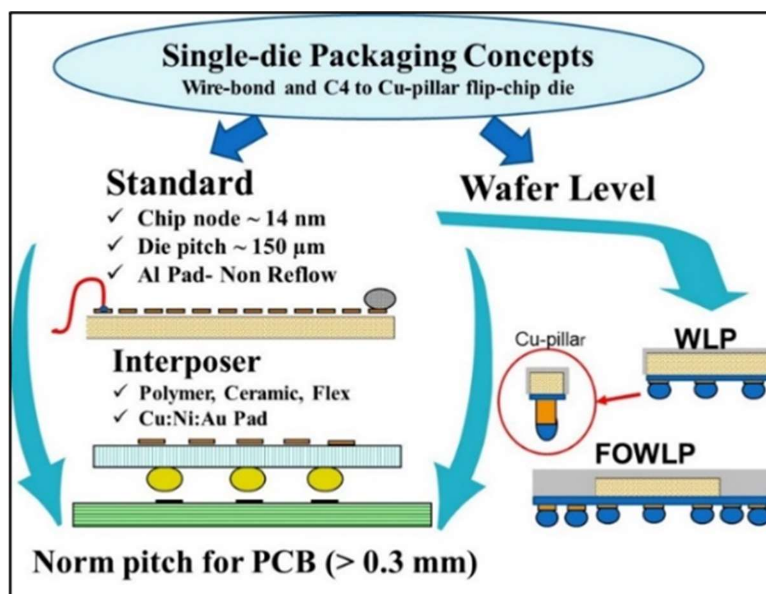

Figure 4-2. Single-chip packaging concept from wire-bond to flip-chip ball grid array to wafer-level packaging (fan-in and fan-out) with C4 (controlled collapse chip connection) and Cu/µCu-pillar with solder tip bumps.

The following presents detailed information on the three device types which were evaluated, e.g., die-size BGA, copper-pillar flip-chip die (CP-FC) and Wafer Level Package (WLP). It shows part type, size, pitch, and number of lands, balls, and copper pillars that were designed in preparation for assembly and subsequent reliability testing. The following list shows the part parameters that are considered as part of a larger DOE implementation.

1. Chip-Array® Ball Grid Array (CVBGA), peripheral array with 360 balls and 0.4 mm pitch with either lead-free or tin-lead solder balls, four daisy chain patterns on each PCB.
2. Embedded wafer level package (eWLP) with 196 land patterns, 0.4 mm pitch, 5.56 mm^2, and 0.5 mm thick, 12 daisy chain patterns on each PCB.

3. CP-FC (CC80) Copper pillar flip-chip die with SnAg solder bump, total of 1048 bumps, peripheral 648 and center full array 400 with 80 μm and 300 μm pitches, SiN diced die 7.3 mm^2, four daisy chain patterns on each PCB.

Figure 4-3 shows optical photomicrograph of Cu-pillar SiN flip-chip die. Visual inspection was performed using standard optical microscopy to determine the integrity of the flip-chip die; but it was difficult to inspect for fine features, as those shown in the figure using an optical microscope with high magnification capability. This microscope also allows measurement of the size of Cu-pillar and traces as images shown in the figure. For a better characterization, scanning electron microscopy should be used to better determine fine features of the Cu-pillar flip-chip die.

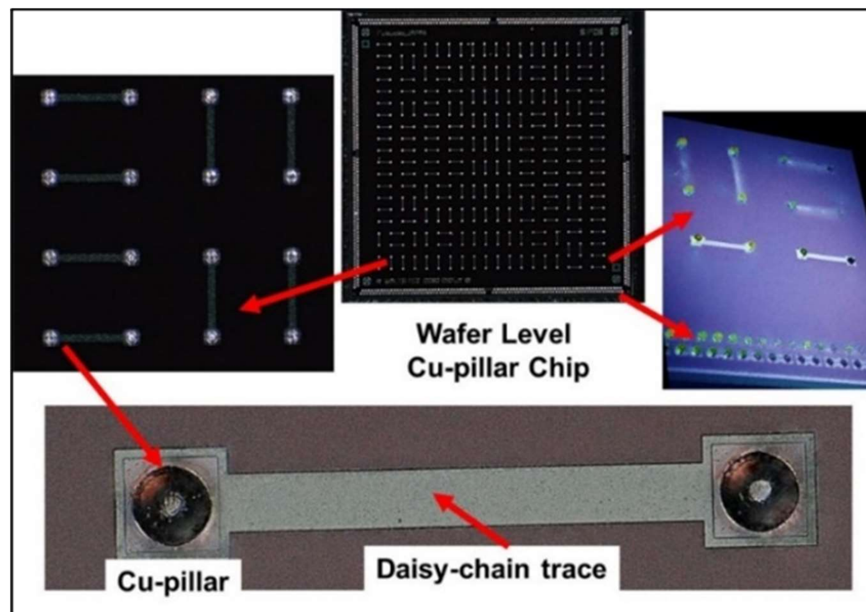

Figure 4-3. Optical images at high magnification showing 3D TSV Cu-pillar flip-chip die and daisy chain patterns with measurement.

4.3 ASSEMBLY AND INSPECTION PROCESSES

Thirty test vehicles with various processing parameters were initially planned for assembly, but it could not be fully implemented due to assembly challenges. Both SAC 305 and tin-lead solder paste were used with subsequent underfill if required. Pastes were printed using an appropriate stencil thickness and aperture. For example, for eWLP-LGA, a 3 mil stencil with 8 mil round aperture opening was used for either tin-lead or SAC solder paste print with subsequent appropriate reflow. Figure 4-4 shows two reflow profiles, the left image for SnPb and the right image for SAC solder alloys.

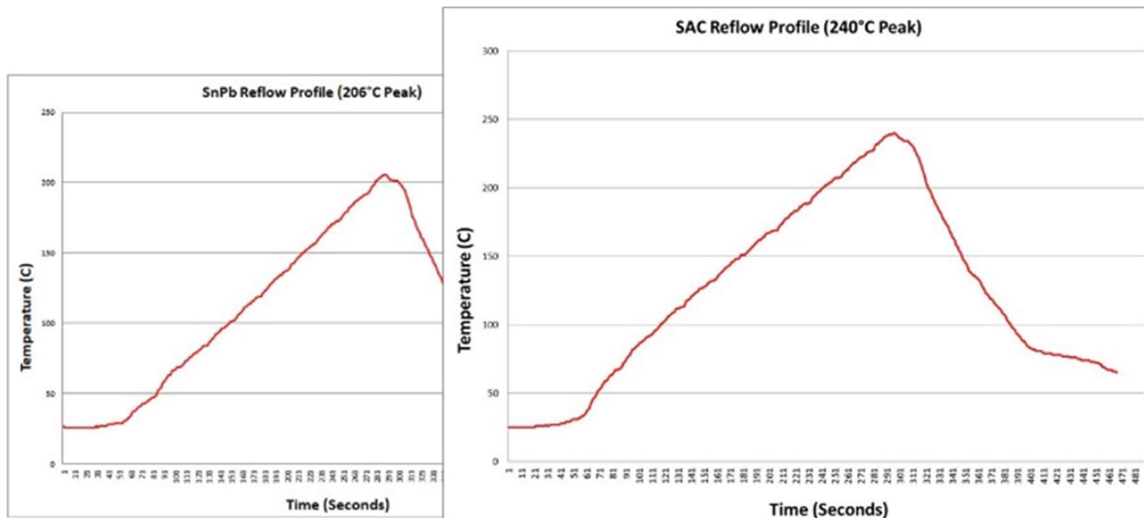

Figure 4-4. Example of tin-lead and lead-free solder paste reflow SnPb reflow profile. Photos are overlapped to show relative maximum reflow temperatures. For SnPb, direct ramp to 206˚C at 0.75˚C/s, -1.4˚C/s cooling rate. For SAC reflow profile, direct ramp to 240˚C at 0.83˚C/s, -1.7˚C/s cooling rate.

The test matrix covered single- or double-sided solder alloys (SnPb and SAC), paste print features, reflow process, and underfill conditions. The basic process flows used to construct and evaluate the test assemblies were:

1. Print solder paste either SAC or SnPb over the printed circuit board for CVBGA and eWLP LGA.
2. Either dip solder flux or solder paste on PCB for CP-FC die.
3. After Paste/Print or flux use an appropriate reflow profile for assembly of the first side of PCB, perform daisy chain verification and X-ray to determine the integrity of first side of assembly and if adjustments to either to paste/flux process or underfilling are required.
4. Reflow followed either with selective underfilling or as assembled in preparation for the second side assembly.
5. Follow steps 1 through 3 in preparation for the top side assembly with subsequent underfill as required.
6. Perform final daisy chain verification test with X-ray inspection.
7. Select those specified for thermal cycling exposures.

Reflow was performed using a convection reflow oven with 10 heating and three cooling zones. All assemblies were inspected by X-ray to characterize the quality of the solder joints prior to environmental exposure. Figure 4-5 shows representative examples of X-ray images for three types of package styles. The X-ray inspection was primarily focused on characterizing voids in the solder joints and identifying solder bridging, if any. Low solder paste workmanship was another defect that was detected, which is associated with LGA having no solder balls, and solder joints are formed through the melting of solder paste.

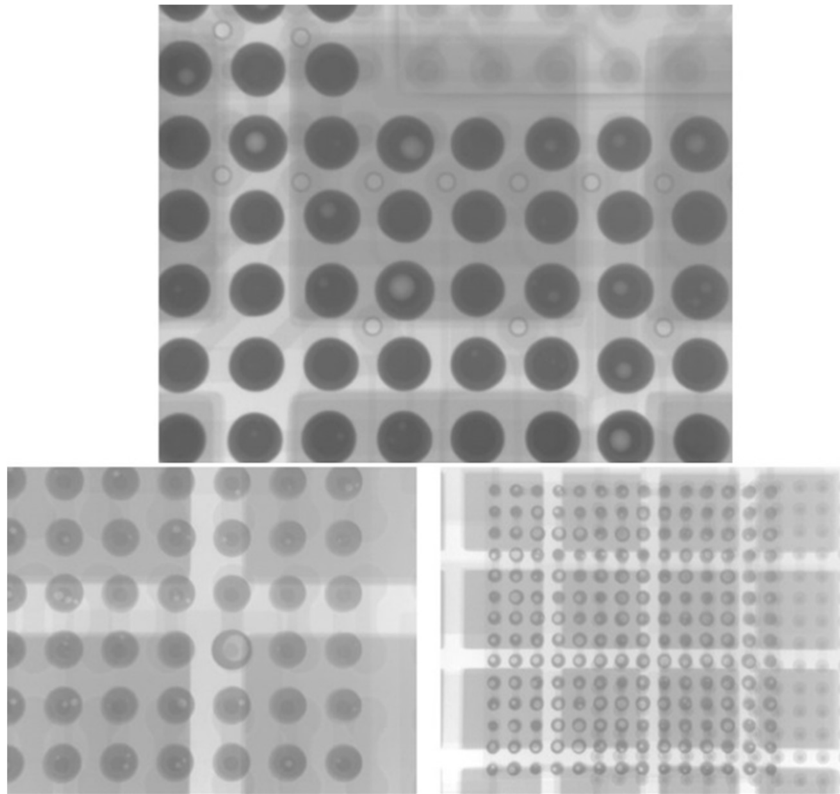

Figure 4-5. Examples of tin-lead and lead-free solder paste reflows showing signs of voids.

4.4 ASSEMBLY PROCESSES MODIFICATION REQUIRED

The first board (TV#1) was processed using a dip flux of about 1 mil (25 micron) depth for CC80 placement. It was reflowed to 210˚C peak temperature, but all CC80 devices fell off the board after reflow. So, flux dip was abandoned for CC80 assembly since there was insufficient solder on the tips of the copper pillars for a dip process to be effective.

The second test vehicle (TV#2) was processed using solder paste. SAC water-soluble, lead-free solder paste was printed using a 4 mil thick stencil on the topside of the board at the CC80 footprints. Stencil apertures were 7 mil rounded squares. The CC80 devices were placed and reflowed to 240˚C. Only three of the four CC80 devices passed electrical inspection after reflow. The board was flipped and SnPb solder paste was printed on the eWLP, CVBGA and CV-LGA footprints. The board was then reflowed to 211˚C. All eWLP-LGAs, CVBGAs and CV-LGAs passed electrical inspection. Only one of the remaining three CC80 devices survived the second reflow. The board was then used for underfill process development. Underfill was dispensed and then cured at 125˚C for two hours. After curing, the previously surviving CC80 device showed daisy chain open.

The TVs 3 through 8 were processed similarly to TV #2, with the exception of using an 8 mil round aperture stencil for the CC80. A second underfill process was added for the eWLPLGA, CVBGA, CV-LGA, and CC80 devices. A number of CC80 devices failed after the first reflow process with more failures after the second reflow. Six of the CC80 devices survived the entire process. Three

CV-LGA failures were due to a small solder deposit formed on a 3 mil thick stencil with 10 mil round aperture (see Figure 4-6).

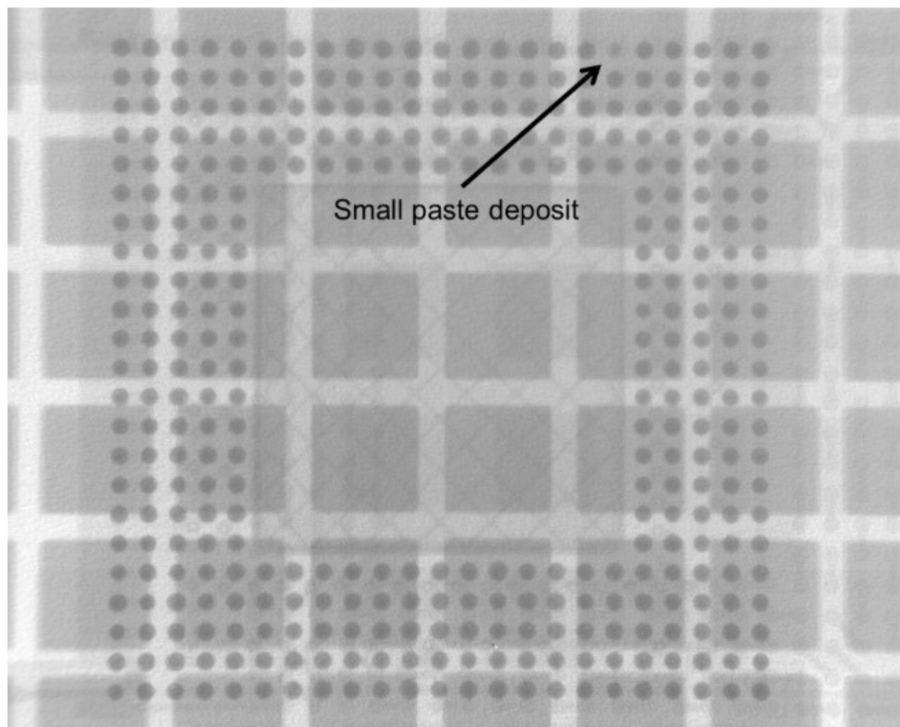

Figure 4-6. An X-ray image of a failed CV-LGA after assembly. As marked, the failure was due to a small solder deposit formed by 3 mil thick stencil with 10 mil round aperture.

Test Vehicle 9 was processed by printing, placing and reflowing the CC80 devices (SAC) and then assembling the eWLP-LGA, CVBGA, and CV-LGA on the same side as the CC80 using a SnPb process. We did not reflow the second side in order to avoid an inverted reflow on the CC80. The three CC80 devices all passed the first (SAC) reflow, but failed after the second (SnPb) reflow.

However, the TVs 10 through 12 were processed with additional underfilling. They were processed by printing, placing and reflowing the CC80 devices (SAC) and then underfilling and curing the CC80 assemblies before performing the second (SnPb) reflow process for the eWLP-LGA, CVBGA, and CV-LGA devices. No second underfill process of the eWLP-LGA, CVBGA, and CV-LGA. Interestingly, 10 of 12 CC80 devices survived this procedure. However, two eWLP-LGAs had failed daisy chains. One was due to a small solder deposit and one was due to a placement error prior to reflow (see Figure 4-7).

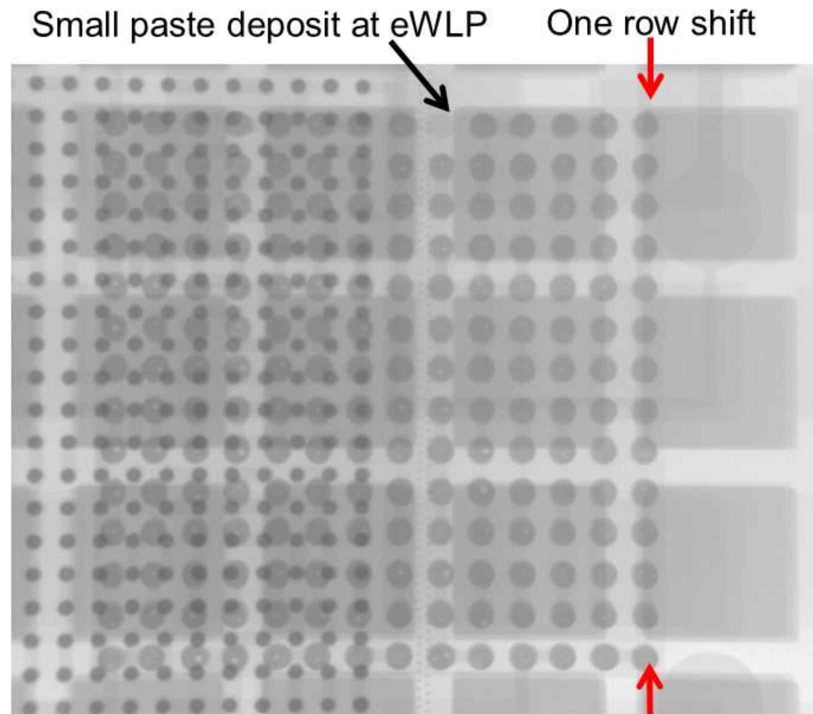

Figure 4-7. X-ray images for the failed daisy chains eWLP-LGAs. One failure was due to a small solder deposit and the other one was due to a placement error prior to reflowing.

TVs 13 through 15 were processed similarly to TV 10 through TV 12, but with the additional step of underfilling the eWLP-LGA, CVBGA, and CV-LGA assemblies. Only seven of 12 CC80s survived the process. There was one eWLP-LGA and one CV-LGA failure. Failures were possibly due to variability of solder paste volume (see Figure 4-8).

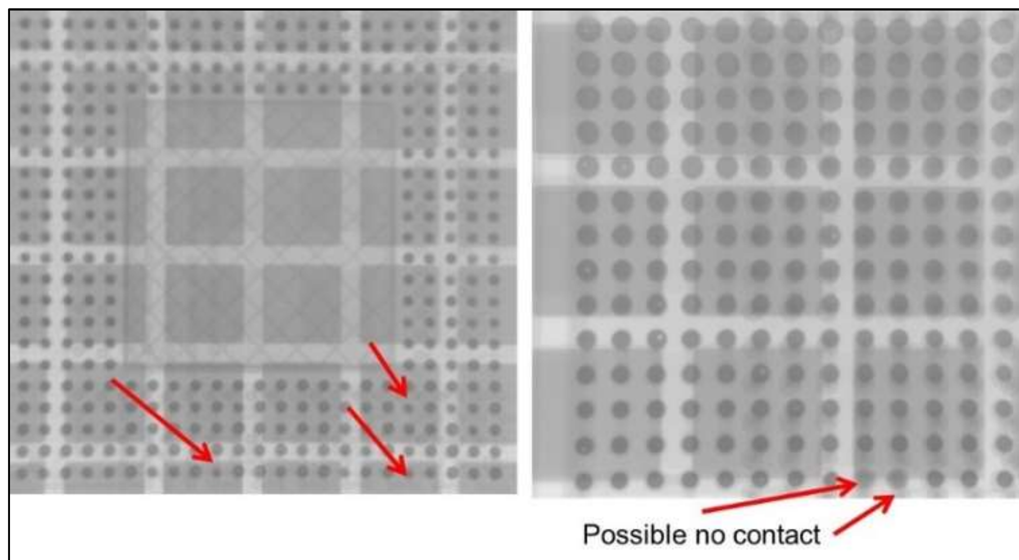

Figure 4-8. X-ray images of CV-LGA (left) and eWLP-LGA with daisy chain opens. As marked, failures were possibly due to variability in solder paste volumes.

Test Vehicles 16 through 21 were processed with a 4 mil stencil and 9 mil square openings for the eWLP-LGA, CVBGA, and CV-LGA in order to increase solder paste volume and possibly to eliminate the workmanship defects due to undersize deposits. Ten of 24 CC80s failed. There were four eWLP-LGA failures due to misplacement.

TVs 22 through 27 were single-sided assemblies using lead-free solder pastes. All parts placed onto PCB. There was one reflow and one cure process. Two CVBGA devices failed due to solder bridging (see Figure 4-9).

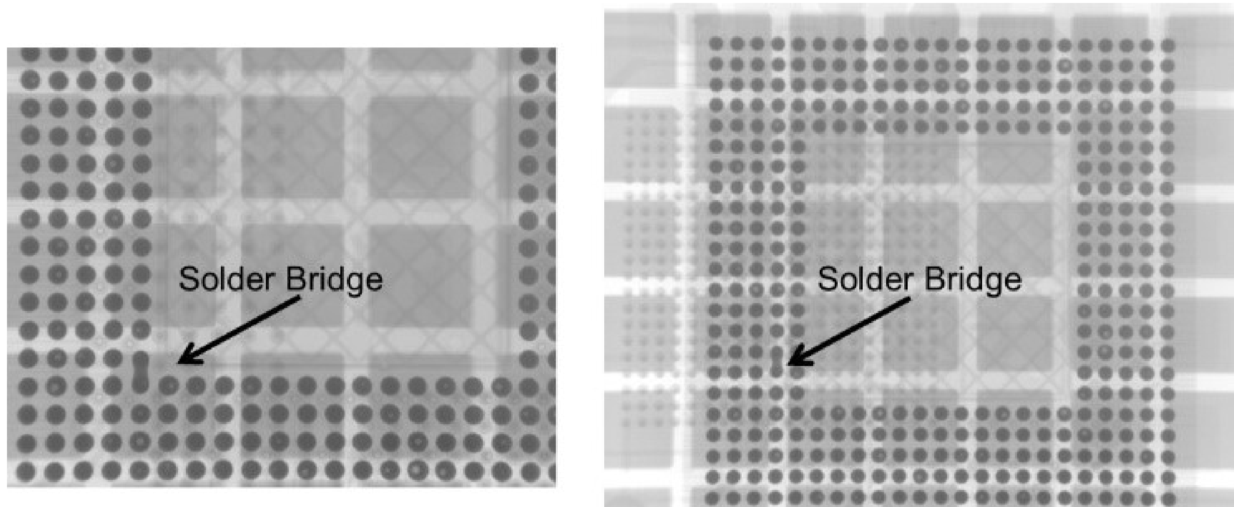

Figure 4-9. X-ray image of CVBGA, as marked both show solder bridging.

5 DSBGA THERMAL CYCLE AND FAILURE ANALYSIS TEST RESULTS

5.1 THERMAL CYCLE PROFILE

Ten lead-free assemblies with SAC 305 solder joints were subjected to accelerated thermal cycling to evaluate reliability. During thermal cycling, an event detector was used to detect daisy chain resistance spikes, exceeding 500 ohms and lasting in an excess of 200 nanoseconds per IPC 9701 capturing failures. Accelerated cycling was performed between -40°C and 125°C with 15-minute dwells at the temperature extremes with a total cycle of 74 minutes per cycle.

5.2 THERMAL CYCLE TEST RESULTS/DISCUSSION FOR CC80

The cycles to failures for CC80 assemblies were extremely poor. As discussed in the previous section, not only was the PCB design challenging and required modifications to accommodate fine pitch requirements, their assemblies also encountered numerous processing issues. The majority of CC80 assemblies failed early just after assembly. In addition, those assemblies that had not failed after assembly failed early in thermal cycling. Only two showed failures at slightly higher number of 85 and 79 cycles. The rest failed even at earlier cycles (11 and lower).

The CC80 early failures clearly show that direct die attachment onto PCB is not a feasible approach with the current PCB technology− even with modification of pad size to enable ease of daisy chain device assembly. Ceramic/inorganic interposer may be required for a mixed technology implementation.

For failure analysis, it is considered that dye-and-pull may not provide sufficient information because of CC80 die being fragile and having a fine feature of copper pillar. For SiP flip-chip die with solder balls, however, we were able to perform dye-and-pry failure analyses [23]. Failure analysis for CC80 was performed by micro-sectioning since it allows precise identification of location of fracture interface in a sectioned plane.

Figure 5-1 shows an overall and magnified optical image of a micro-sectioned CC80. It shows that even though solder balls are formed surrounding the copper pillar pins, failures generally occurred at the interfaces. Copper pillar had a thin layer of SnAg, which may not have been sufficient to form an adequate metallurgical bond at its interface. The SnAg may not have melted during soldering reflow and therefore its interface may have been separated to begin with. If the tip is oxidized, it will also prohibit adequate interfacial bonding. Further investigations are required to narrow the root cause of interfacial failures.

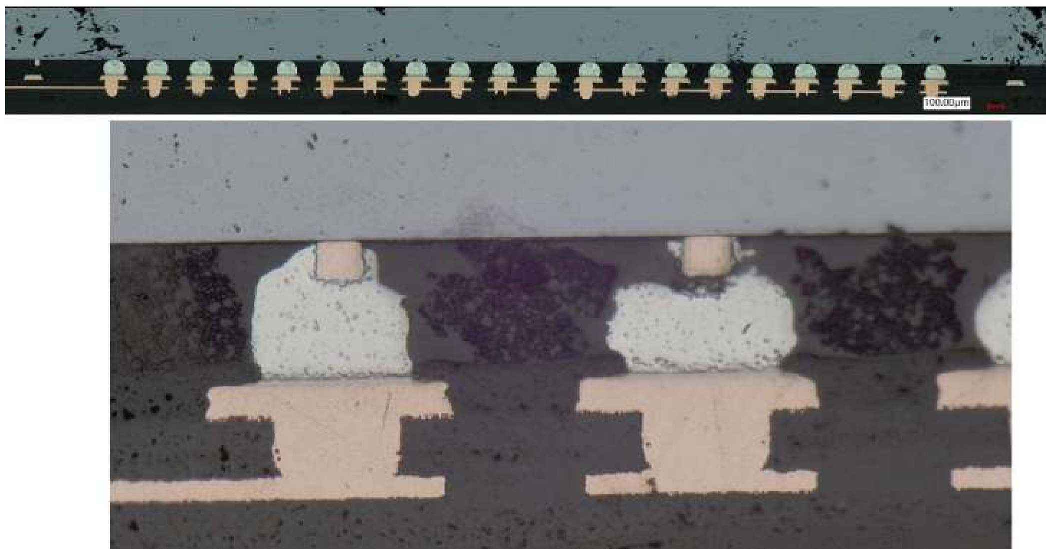

Figure 5-1. Microsection images of thermal cycle CC80 showing a failure mechanism to be at the copper pillar to solder joint interface. Note the use of microvia to accommodate the fine pitch daisy chain pattern of CC80.

5.3 THERMAL CYCLE TEST RESULTS/DISCUSSION FOR EWLP-LGAS

Table 5-1 shows the thermal cycle test results for eWLP-LGA assemblies without and with underfill conditions. Even though assembly of this package was less challenging compared to CC80, it is less robust because it is in a land grid array configuration. A quick scan of cycles-to-failures test data reveals that those without underfilling failed earlier than those with underfilling. To establish the trend, accumulation of failure percentages was plotted versus the number of cycles as shown in Figure 5-2.

For non-underfills, the eWLP-LGAs failed in a narrow range of 74 to 170 cycles while underfill assemblies failed in a very wide range of 311 to 1524 cycles. The Weibull β parameter, which represents a higher spread in data with a lower value were 6.27 and 3.88, respectively. Their Weibull η values were 132 and 656 cycles with correlations of 0.97 and 0.86, respectively.

Failure analyses were performed by removing assemblies at appropriate times to determine failure mechanisms, which ideally should be within bulk or at interfaces within solder joints. Figure 5-3 shows a representative cross-sectional microscopy of a test vehicle at location B2 removed after 951 cycles for failure analyses. In contrast to CC80, eWLP-LGA failed within solder joints as is apparent from the X-sectional images. However, the apparent solder joint coarsening may not have been there at the time of failure since the assembly had been exposed to additional thermal cycles.

Table 5-1. Number of cycles to failure for eWLP-LGA assemblies with and without underfill.

		eWLP (.4mm pitch) LAND GRID ARRAY											
		B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
BARCODE	**2nd underfill pass**	**Microvia-2nd Layer Trace**						**Surface Trace Only**					
brd713635	Underfill except B3, B4,B5,B6, B11,B12	714	549	**91**	**159**	**123**	**118**	882	632	777	902	**113**	**102**
brd713638	eWLP-LGA	380	511	539	455	311	488	712	758	680	340	464	485
brd713642	eWLP-LGA	422	491	425	375	590	329	458	459	411	343	417	486
brd713648	eWLP-LGA	394	715	403	624	642		827	602	625	936	874	539
brd713654	eWLP-LGA	431	543	393	474	401	512	618	499	623	500	463	491
brd713641	None	74	134	146	120	122	160	140	144	124	141	159	136
brd713645	None	104	158	84	146	92	146	121	93	143	99	164	117
brd713651	None	97	122	94	135	93	149			132	88	135	170
brd713656	None	134	117	106	87	124	119	116	150	119	117	129	112
brd713658 Underfill 1St Side All	None	741	1262	839	1142	601	447	377	851	860	791	838	1524
		No Underfill for those with red mark at the top right corner											

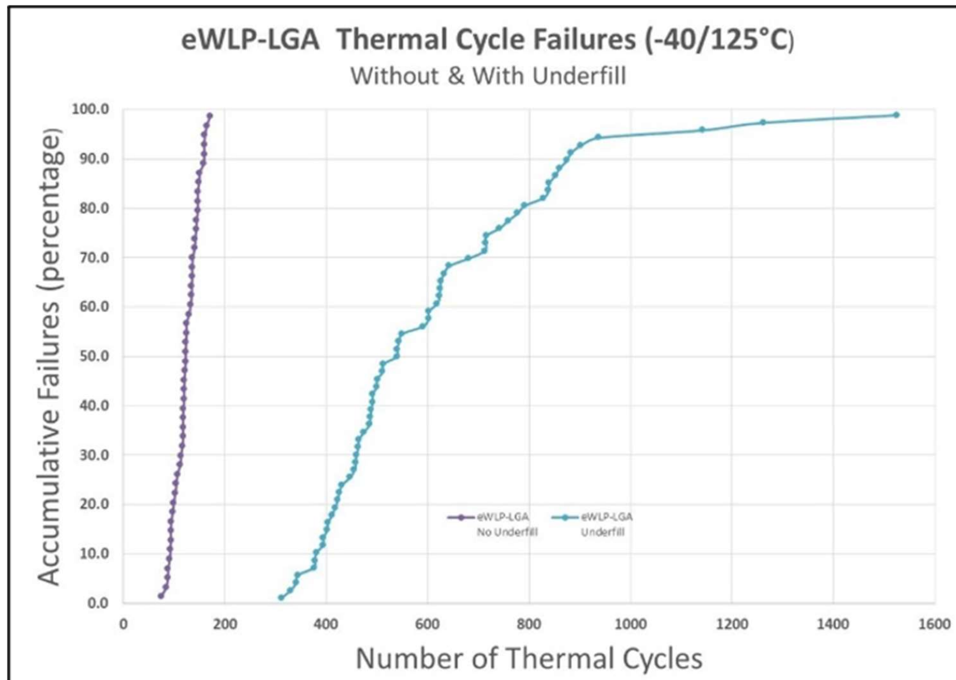

Figure 5-2. Accumulative cycles-to-failures for eWLP-LGA assemblies without and with underfill. The Weibull β parameters were 3.88 and 6.27 with η values of 132 and 656 cycles, respectively.

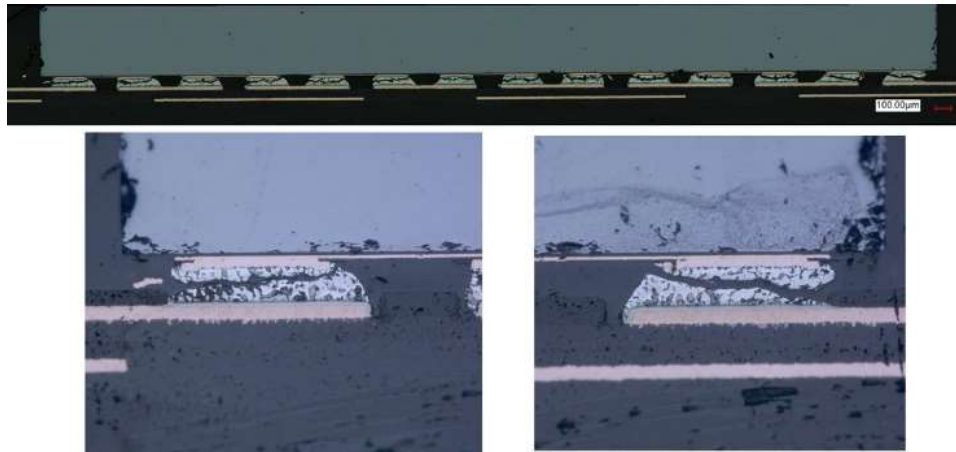

Figure 5-3. Representative micro-section images showing early failure of eWLP-LGA at B2 location of Bar Code 713651 PWA removed after 951 cycles and X-sectioned.

5.4 THERMAL CYCLE TEST RESULTS/DISCUSSION FOR CV-LGA AND CVBGA

Table 5-2 shows the thermal cycle test results for CV-LGA and CVBGA assemblies with and without underfill conditions. The assembly of land grid array version of this package, CV-LGA, was challenging similar to its eWLP-LGA counterpart; it also showed the lowest cycles-to-failures. However, CVBGA was not only easier to assemble, its underfill version showed no-failure to 3,000 cycles when cycling stopped.

Figure 5-4 shows cycles-to-failures for the four assemblies, the lowest for CV-LGA, which improved with underfill. The no-failures were for CVBGA with underfill. CVBGA without underfill failed between CV-LGA without and with underfills, The Weibull β and η parameters with their correlation for CV-LGA/BGA cycles-to-failures are:

- CV-LGA without underfill:

$\beta = 6.625$, $\eta = 553.456$, R2 = 0.9669

- CV-LGA with underfill:

$\beta = 5.761$, $\eta = 929.719$, R2 = 0.9646

- CVBGA without underfill:

$\beta = 2.819$, $\eta = 709.256$, R2 = 0.9360

- CVBGA with underfill:

Note: No Weibull parameters since no-failures to 3,000 thermal cycles.

The Weibull β parameter, which represents a higher spread with a lower value in data was 2.8 for CVBGA without underfill condition. Interestingly, the CVBGA failures spread between CV-LGA without and with underfill conditions. There was no failure of underfilled CVBGAs, a substantial improvement which is a critical parameter for high-reliability applications.

For comparison to eWLP-LGA, a CV-LGA was cross-sectioned for failure analyses. Figure 5-5 is an image of this assembly with early failure. Similarly, an overall with two corner solder joint images taken at a higher magnification is shown for comparison. This is for location at A2 from the assembly with Bar Code 713651, which was removed at 951 cycles. This CV-LGA failed at 555 cycles as shown in the table. Failures are within solder joints close to the top of package, which is different from eWLP-LGA with failures across the diagonal of solder joints, possibly due to its lower height of solder joint due to using only solder paste.

Table 5-2. Number of cycles to failure for CVBGA and CVLGA assemblies with and without underfill.

		CVBGA (.4mm pitch) (SnPb or LGA)			
		A1	A2	A3	A4
BARCODE	2nd underfill pass	Microvia-2nd Layer Trace		Surface Trace	
brd713635	CVBGA/CVLGA	>3000	***922***	>3000	***718***
brd713638	CVBGA/CVLGA	>3000	***749***	>3000	***800***
brd713642	CVBGA/CVLGA	>3000	***568***	>3000	***996***
brd713648	CVBGA/CVLGA	>3000	***990***	>3000	***1049***
brd713654	CVBGA/CVLGA	>3000	***1031***	>3000	***810***
brd713641	None	351	***526***	1106	***389***
brd713645	None	385	***549***	827	***471***
brd713651	None	327	***555***	801	***622***
brd713656	None	569	520	726	724
brd713658 Underfill 1St Side All	None	>3000	>3000	>3000	>3000
		Orange Box (*Italic* /**Bold**) LGA version of CVGA			

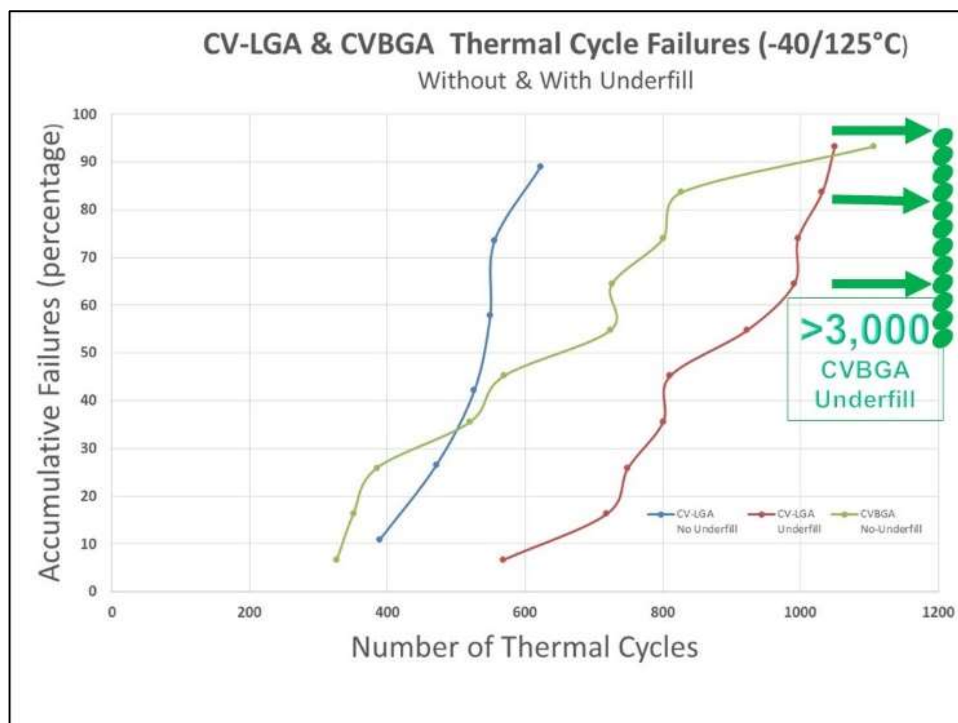

Figure 5-4. Cycles-to-failures for four CV (BGA/LGA) assemblies, the lowest for CV-LGA, which improved with underfill. The highest values for CVBGA with underfill showing no failure to 3.000 cycles.

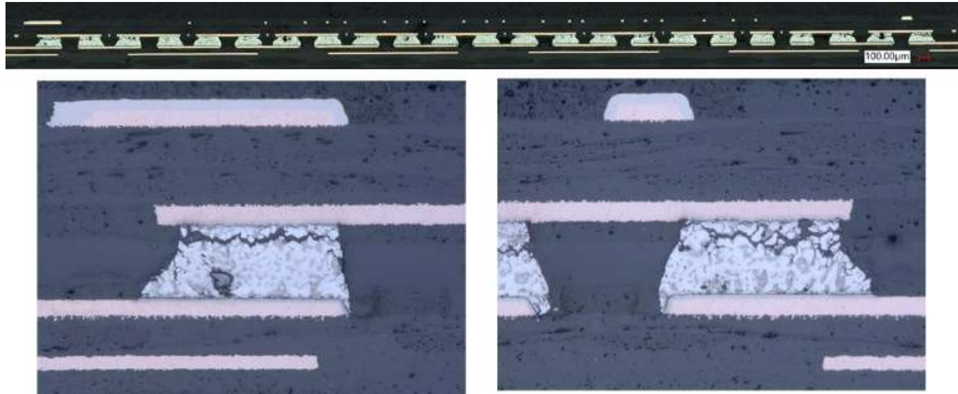

Figure 5-5. Representative failure of CV-LGA at A2 location for Bar Code 713651 assembly, which removed after 951 cycles and then X-sectioned.

6 NASA APPLICATION: BGA/DSBGA

6.1 PURPOSE AND RECENT FINDINGS ON COTS

This guideline document presented the key aspects of COTS packaging technologies with examples from two NEPP projects on BGAs and DSBGAs that were recently evaluated to complement lessons learned on this subject. The two NEPP tasks covered detailed methods for assembly, inspection, and reliability characterization evaluation that could be used as guidelines for establishing thermal cycle reliability for new advanced ball grid array packaging technologies. Test evaluations with the number of thermal cycles to failures were presented for wire-bond BGAs as well as FCBGA. It also presented detailed characterizations of DSBGAs technologies and their land grid array versions with and without underfilling conditions. The NASA application section summarizes not only lessons learned from the two NEPP tasks, but also presents a literature search and lessons learned from the author's experience; practical lessons learned from implementation of array technologies for NASA spaceflight projects.

Use of COTS at the NASA Centers was the subject of a recently published NESC report [25]. It included key findings on the COTS current practices, best practices, lessons learned, and their recommendations. Specifically, it covered use of electrical, electronic, and EEE COTS parts for spaceflight systems as well as use of EEE COTS parts and assemblies in critical ground support equipment (GSE), and provided a number of specific examples for applications. It recommends selecting COTS parts from Industry Leading Parts Manufacturers (ILPMs) that meet a specific project's MEAL requirements [26]. The author's review of this NESC report shows that a number of lessons learned on COTS, dispersed within the report, are relevant to generic aspects of this BGA/DSBGA guideline that emphasizes the board level assembly, quality, and reliability implementation. Key examples of NESC findings are shown in the following list.

1. COTS parts could be overstressed when screened per Mil-Spec/Space specifications without considering the maximum temperature limitations of the COTS parts. Over-stressed parts could fail at assembly level, where risk of rework is also high. The COTS glass transition temperature and pre-condition should be also addressed.
2. COTS "part issues" are mostly not associated with the parts; the likelihood of other issues is much greater than an actual part defects or failures. Other issues include workmanship, solder shorts, thermal design, cold solder joints, design deficiency, incompatible connectors, improper derating, worst-case analysis deficiency, etc.
3. COTS assemblies could fail under shock and vibration due to their miniature sizes, e.g., small size connector.
4. COTS BGAs and LGAs could fail under mechanical shock and vibration. These either had to be replaced or the board had to be stiffened by increasing board layer counts and/or adding aluminum stand-offs around the parts. Mechanical shock absorbing materials sometimes had to be added in the system assembly in order to pass the shock and vibration tests.

In the following, the author addresses specific key uses of COTS BGA/DSBGA packaging technologies at the assembly level with consideration of NASA MEAL requirements based on years

of NEPP research activities on this subject and years of reliability characterization of electronics hardware assemblies for spaceflight applications.

6.2 MISSIONS & BGA/DSBGA APPLICATIONS

This guideline categorizes BGA technologies from their application robustness, e.g., BGAs or DSBGAs, as well as generically categorizes a number of NASA's MEALs, e.g., short-time and benign or long-time and extreme, with the risk posture of mission in order to better narrow recommendations on use of COTS BGAs/DSBGs for numerous mission scenarios. Figure 6-1 summarizes the key aspects of BGAs/DSBGAs technologies discussed in this report. It features the following aspects:

1. BGAs with internal wire bond; either gold or copper wire bond with either single or multiple stack wire bonds. Outer solder balls could be tin-lead or various lead-free solder alloys.
2. FCBGA with internal high-lead or tin-lead eutectic solder balls as well lead-free solder balls. Copper-pillar with solder bump at tip are a new flip-chip interconnection. All come with underfilled die. Outer BGA balls for board assembly are either tin-lead or lead-free solder alloys.
3. DSBGAs' internal die and interconnections are unique; therefore, it is classified based on pitch and robustness at assembly level without and with underfill. The outer balls are considered tin-lead, lead-free, and land pad only.

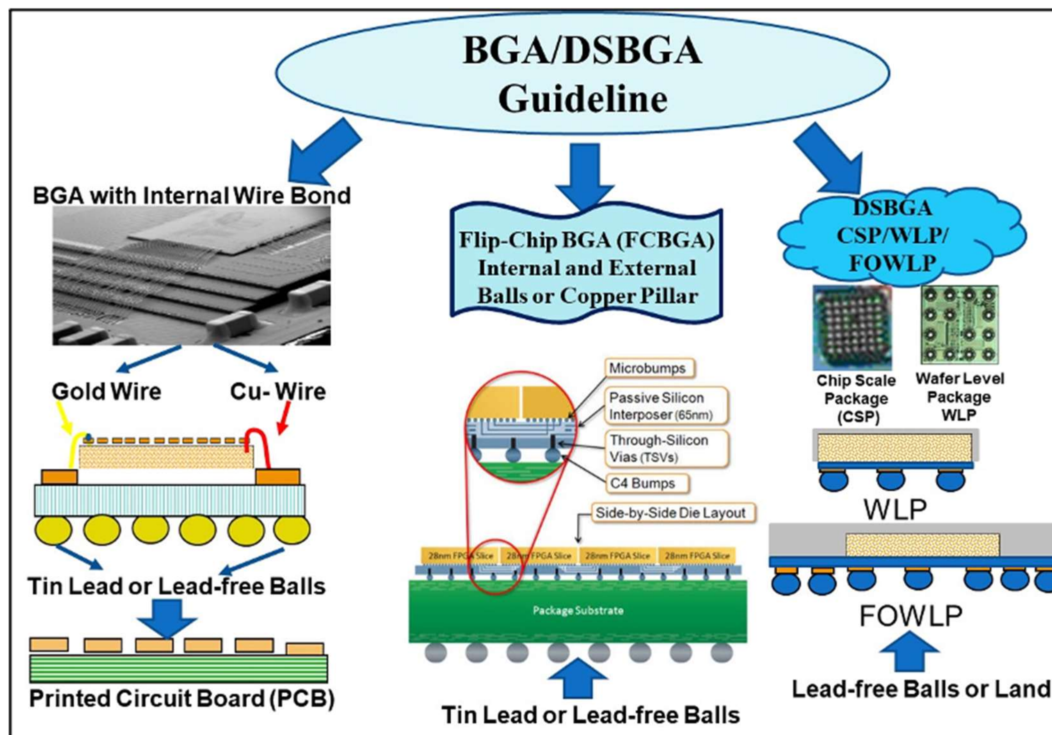

Figure 6-1. Three Key BGA, FCBGA, and die-size BGA technologies covered in this guideline document.

Each spacecraft has a unique MEAL even for each instrument that needs to be addressed appropriately. A MEAL for each instrument is required to be uniquely defined within spacecraft requirement and risk posture. For example, Figure 6-2 shows complexity of a MEAL requirement for M2020 Perseverance Mars Rover with each instrument having a unique MEAL requirement and risk posture acceptance. Therefore, it is extremely difficult to address reliability based only on an overall risk posture of a class mission type, but it should also include numerous aspects of each instrument reliability requirement. This makes it difficult to generalize MEAL requirements, but there was an attempt to address them in the following with understanding of these deficiencies.

Reviewer, Dr. John Evans [27] states, "I agree. There is a lot of nice test data but it needs to be related to mission conditions. There are a variety of missions that these technologies will need to serve. I think we need an approach to relate the test information to each mission. Generalizing will not cover the real mission conditions." So, if mission details are known, use them.

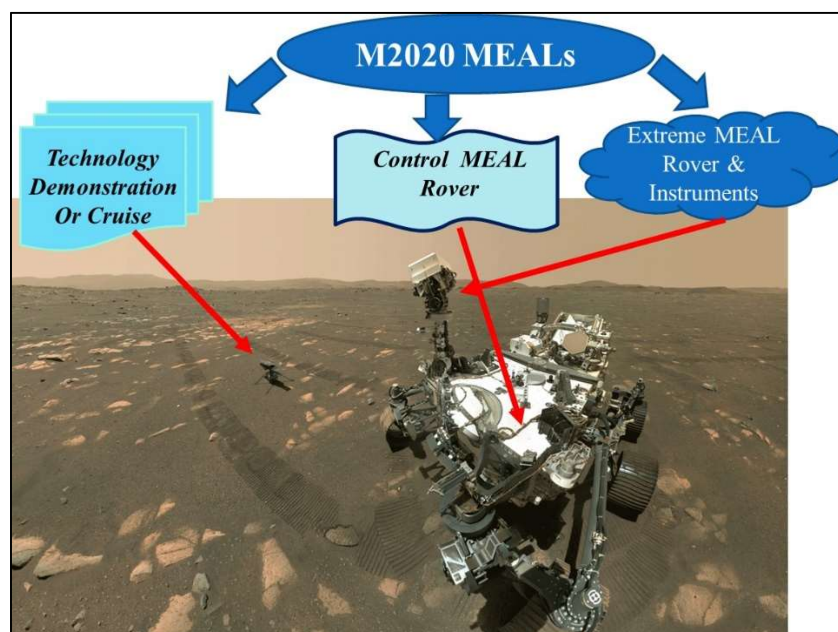

Figure 6-2. Various instruments of M2020 Perseverance Mars Rover showing complexity of implementation of MEALs requirements.

Nevertheless, to start at a baseline, general recommendations are provided below for BGA/DSBA applications. The mission types and risk postures are simplified to the following categories.

1. Low Risk Posture, Class A and B.
   a. Moderate or Extreme MEALs, short and/or long-time missions.
2. Medium to high risk posture, Class D and Sub D.
   a. Benign MEALs, short- and/or long-time missions.

With consideration of MEAL requirements, each level of integration should be considered because of different requirements for each level of integration. Furthermore, to narrow evaluation approaches at each level, the capabilities, advantages, and limitations of testing and inspection

should be considered. Risk incurred by omitting a verification step depends on the level of integration as well as MEAL requirements for the specific electronics hardware. A clear understanding of the different verification processes is needed to ensure the proper verification of the BGA/DSBGA packaging technologies. The testing could follow the current conventional piecewise qualification approaches for EEE parts, or a holistic approach of using electronics hardware at assembly and box level, especially when a large number of hardware is available for higher level testing.

In the following, guidelines will be provided first for selection of COTS BGA/DSBA part/package and then parameters for their assembly optimization, and especially improvement in solder joint reliability for spaceflight applications.

6.3 BGA/DSBA PACKAGE CONSTRUCTION REVIEW

Prior to design, it is recommended to review numerous NASA, military, and industry standards on this subject, including IPC 7095, Design for BGAs, IPC 7094, Design for Flip Chip, and IPC 9701, Qualification and Performance for SMT, and NASA-STD-8739.1 for Polymeric Applications. In addition, it is recommended to gather the following information:

- Define the overall NASA mission environmental requirements and risk posture, including radiation, mechanical, thermal, life cycle, mechanical shock, vibration, etc.
- Perform appropriate accelerated environmental tests, representative of environmental requirements, to reduce the time to failure and understand failure mechanisms. For example, in thermal cycle tests, the larger the ΔT, the shorter the time to failure of BGA/DSBGA solder joint assemblies. Failure mechanisms should be representative of smaller ΔT flight fluctuations.
- Narrow potential COTS packaging technologies and types using supplier data and application notes. Packaging technologies include: COTS high I/O flip-chip BGAs, low and high I/O wire-bond BGAs (gold/Cu with coating), and fine pitch DSBGAs. Review build up, materials, solder geometry and solder alloys (internal or external), heat distribution, etc.
- Determine solder alloy of solder balls for BGA/DSBA since industry has now widely implemented use of numerous lead-free solder alloys. This is critical for compatibility with tin-lead solder during assembly solder reflow that also affect solder joint reliability under thermo-mechanical loading as well as resistance to mechanical shock and vibration.
- Look for vent holes in BGA and mitigation, if applicable. Small vents generally are deliberately designed between the heat spreader (lid) and the organic substrate to allow for outgassing and moisture evaporation during the cleaning process. These vents themselves, however, become a reliability issue. Cleaning solvents and other corrosive chemicals seeped through these vents, and they attacked the organic materials and components inside the BGAs. Recently, package supplier's application notes address the vent issue.
- Address reliability concerns for flip-chip polymeric underfill and adhesively bonded heat sink for non-hermetic FCBGAs. During the assembly processes, exposure of polymeric underfill to cleaning solvent/chemicals or excessive moisture could pose serious packaging issues since polymers are sensitive to such exposure.

- Review application notes carefully for any design that will later exacerbate the condition, either during initial package burn-in thermal evaluation or subsequently during manufacturing. Examples are die exposure to aggressive cleaning through venting hole or damage to FCBGAs underfill due to cleaning agent or long-time high temperature exposures.
- Evaluate by X-ray and construction analysis the composition of internal wire bond composition. Gold wire-bonded BGA/DSBGA Packages are widely evaluated and more reliable because the interconnections have stress relief. Copper wire bonds with and without coating are now widely implemented by industry. In general, wire-bonded devices should be selected if available and meet functional requirements.
- Review construction of BGA/DSBGA since flip-chip die reliability robustness of FCBGA depends on solder ball size and alloy as well as underfill type. Copper pillar is a newer technology. All parameters should be reviewed for reliability integrity.
- Determine if the effect of high-temperature burn-in on reliability is evaluated. Burn-in is a requirement for high-reliability applications and industry does not require that for COTS; therefore, there is limited study on this subject. Determine its effect on reliability.
- Consider the effect of burn-in beyond the part degradation. It not only affects the die behavior, but it also the integrity of BGA/DSBA solder ball joints due to subjecting them to shear or tensile loading under testing. Assembly reliability is affected by degraded solder ball joints at the package pad interface as well.
- Be prepared for challenges associated with electrical verification tests for FCBGA/BGA field programmer array packages since the user has limited access to comprehensive burn-in and electrical tests compared to part manufacturers.
- Review electrical burn-in socket approach for induced stress, especially at high temperatures, could cause damage and/or dislodge/dislocate solder balls. The reliability consequence of burn-in on subsequent assembly is not well established for such conditions.
- Determine if package properties are within the envelope of mission environmental requirements in order to avoid early overstress failures. Examples include radiation capability of die, temperature limits of package materials, including softening temperature (glass transition temperature, Tg), and junction temperature. Determine if special handling, bake out, assembly process, and tools are required.
- Consider other parameters for molded BGA/DSBGA since, in addition to Tg, the filler content of molding compound also has an effect on the thermal cycle reliability.
- Determine the type of substrate (i.e. rigid, flexible) and lay-up and microvia since these parameters affect board level reliability with flexible substrates being more prone to fatigue damage from thermal excursion.
- Include the effect of die size-to-package ratio for thermal cycle test data projection since this ratio influences the thermal coefficient of expansion mismatches under thermal cycling. Solder joint reliability generally decreases with an increase in die-to-package ratio.
- Consider the effect of ball counts on reliability. Thermal cycle reliability of the BGA/DSBGA generally increases with the increase in the ball count of the package since

the stress level in the individual ball is reduced due to distribution of thermal deformation over a larger number of solder joints.

- Consider the effect of solder ball height, including solder column, for reliability improvement. Thermal cycle reliability of BGA/DSBA generally increases with an increase in the package ball diameter since the crack path increases with the ball diameter. The most improvement is achieved by using solder column.
- Review moisture sensitivity and bake out recommendation. BGAs/DSBAs absorb moisture, which can be degraded. They are assigned different moisture sensitivity and bake out recommendations before assembly. See manufacturer recommendation or J-STD-033 or equivalent.
- Provide appropriate control steps based on moisture sensitivity of BGA/DSBA to prevent moisture-induced damage. Control storage may be required including using a Moisture Barrier Bag (MBB), drying cabinet, or nitrogen-blanket.
- Request or perform 3D X-ray imaging to determine internal die assembly workmanship defects including Head-on-Pillow (HoP) for flip-chip die attachment or closeness of wire bond to lid encased BGA with internal wire bond, and wire bond touch due to resonance under vibration.
- Review non-standard PCB technologies for MEAL since a number of modifications are required to accommodate BGAs and especially DSBGAs. These include microvia and stacking vias, surface finish, and pad opening and mask.
- Design Non-Solder Mask Design (NSMD) PCB pads for BGAs, which mask openings larger than the pads. NSMD prevents crack initiation in solder joints whereas Solder Mask Defined (SMD) initiates crack via mask being in proximity contact with solder joint. NSMD reduces solderable pad size.
- Preference is given to SMD for miniature PCB pads for DSBAs, in which the solder mask opening overlaps the copper pad. SMD reduces the likelihood of the pad lifting during the soldering or de-soldering process and it increases the solderable pad size.
- Consider the PCB layup/thickness in reliability projection. Thermal cycle reliability for BGA/DSBGA assembly generally decreases with an increase in the PCB thickness since it affects assembly stiffness. An increased PCB thickness results in higher stresses in solder joints with reduced reliability.

6.4 BGA/DSBGA PCB ASSEMBLY

Limited flight heritage exists for PBGAs/FCBGAs/DSBGAs, especially for Class A/B, even though in most cases packaging suppliers may have generated second level reliability test data and contract manufacturers may have already implemented use of PBGA/FCBGA, though that may not be true for DSBGAs. Generally, the large pitch BGAs have shown to have adequate thermal cycle resistance, but low resistance to shock and vibration, which requires proper strengthening mechanisms. Review heritage and package supplier's data for package- and second-level solder joint reliability. Use the following generic guidelines for meeting the requirements:

- Use of DSBGA should be restricted and only after careful review of vendor data and acceptability, should it be qualified for specific class D applications.
- Use corner fill to determine if it is sufficient to increase shock/vibration improvement to an acceptable level before selecting the option of full underfilling since full underfill may induce unacceptable reduction in thermal cycling resistance.
- Follow manufacturer's recommendation for underfill material and plan to optimize filling process for adhesion integrity and void minimization. Cleanliness and de-moisturization are required for effective underfilling. If dispensing underfill at ambient conditions, it should be accomplished only from one side of the device to ensure that air is pushed out ahead of the adhesive.
- Use a daisy chain package as the test article for accelerated thermal cycle tests as specified in IPC 9701. Daisy chain packages are generally built using similar materials and layup as the functional package with the exception of using a dummy die with even/odd pad connections. Die size affects solder joint reliability and, therefore, should be the same size or larger than the flight-like package.
- Design double-sided assembly if it represents flight configuration. However, note that double-sided, mirror-image assemblies show major reduction in solder joint reliability.
- Optimize mixed solder alloy technology assembly since it is preferred to re-balling with tin-lead solder when the effect of alloying elements is understood and proper reflow processes followed. Pay careful attention to the reflow process to avoid melting of solder balls in order to take advantage of taller non-collapsed solder ball height, which improves thermal cycle resistance in comparison to melted collapsed tin-lead solder balls.
- Non-collapsed solder balls are preferred, or in some cases must be controlled during tin-lead reflow including those with high-lead or SAC solder balls. An example with non-collapse high lead solder balls was presented for 3D Stack BGA in the first test section of this guideline.
- Optimize reflow thermal profile, especially for a mixed technology assembly. Remember that process optimization and process control are key parameters that control solder attachment integrity for area array packages, not optical/visual inspection, as commonly used for most other electronic packaging assembly. Refer to standards for use of acceptable flux, solder paste quality test, and cleanliness requirements.
  - Perform real-time X-ray and optical inspection. 3D X-ray is preferred since it better characterizes solder damage, but it has its limitations. The 2D X-ray system used in this investigation did not reveal the level of solder damage due to thermal cycling.
- Perform optical microscopy and SEM evaluation of the outer rows of package assembly to reveal damage prior to destructive X-section, which is performed to reveal internal damage and crack formation.

6.5 BGA/DSBGA FOR MEAL

For life thermal cycle qualification, determine life cycle requirements for the mission. For the purpose of further narrowing package selection, consider the following four simplified categories of NASA missions:

A. Extreme temperature cycle exposure with long mission duration [James Web Space Telescope (JWST), Camera in Mars 2020, Solar Array for Europa Clipper, etc.].

B. Extreme thermal cycles with short mission duration (Mars Exploration Rover [MER], Spirit and Opportunity, InSight Mars Lander, etc.).

C. Benign thermal cycles with long mission duration (International Space Station, Control environment of James Web Telescope, Mars Rover Warm Electronic Box, Europa Clipper under Control Environment).

D. Benign thermal cycle exposure with short mission duration (e.g., Class D and SubD, Cruise for Mars Mission).

If details on life cycle requirements are not available, then use the following rules of thumb to estimate the number of accelerated thermal cycles (−45°C to 85°C) or specific temperature ranges,

- For A and B missions, estimate the flight allowable temperature ranges and multiply mission cycles by 3. Add at least 10 additional cycles with temperature margin for ground cycles.
- For C and D missions, estimate thermal life cycle requirements based on mission life. The number of thermal cycles are estimated to vary from 50 to 1000 accelerated cycles in the range of −45°C to 85°C for 6 months (~ 50 cycles) and 10 years (~1000 cycles) for about 10 years.

For class A/B, extreme and long-time/extreme MEAL, consider the following recommendations including special qualification approaches. Ensure that all constraints on the use of COTS plastic packages for BGAs and DSBAs are well understood.

- Use equivalent hermetic seal packages such as CQFPs and CGAs or Class Y CGAs.
- Consider using solderless CLGA with interposer to reduce risk of rework. Pay special attention to heat sink attachment and stress relief implementation.
- Avoid pure tin finish. Follow industry guides including those specified in the space addendum of J-ST-001. Develop and implement risk mitigation and reduction methods including dilution with lead, encapsulation of joints, and conformal coating.
- Avoid stack microvia and Via-in-Pad (ViP) for PCB. Single layer microvia requires qualification.
- Avoid exotic PCB surface finish. Use hot air solder leveling (HASL) surface finish. PCB. Perform qualification for use of exotic finish. New ENEPIG is preferred to ENIG PCB finish.

For class A/B, short-time benign MEAL, the following recommendations should be considered including possibly special qualification approaches for meeting the MEAL requirements. However, ensure that all COTS BGA/DSBGA constraints envelope the requirement,

- No pure tin finish is allowed. Implement risk mitigation and reduction methods.
- Microvia and stack microvia and ViP for PCB may be acceptable. Single layer microvia is preferred.
- Exotic PCB surface finish may be used if needed including ENEPIG.

Figure 6-3 presents an example of potential application with restriction of COTS BGA/DSBGA for M2020, of which the author is familiar, but similar approaches should be considered for other spacecrafts. MEAL divided into three key thermal cycle requirements: (1) Technology demonstration, e.g. Ingenuity Helicopter and Cruise, (2) Control environment for electronics, and (3) Extreme environment, those directly exposed to Mars environment, e.g., camera and high gain antenna.

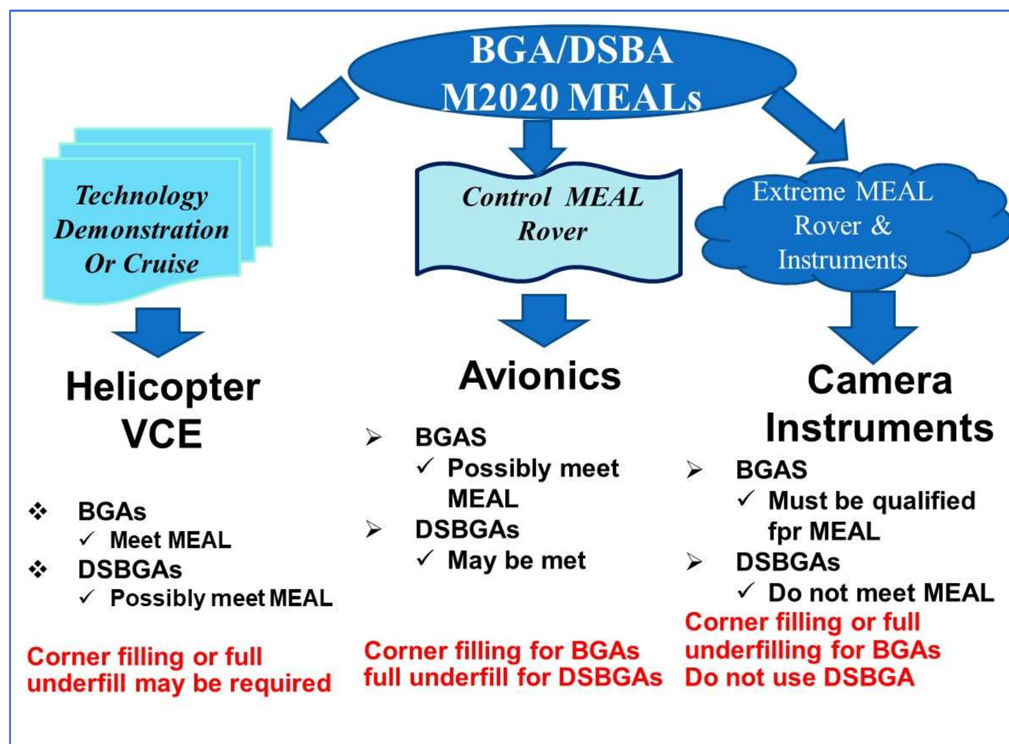

Figure 6-3. MEAL for COTS BGA/DSBGA if they were considered for M2020 Perseverance Mars Rover and Ingenuity Helicopter, a technology demonstration, on Mars.

6.6 MEAL BGA/DSBA ASSEMBLY TESTING

Figure 6-4 presents a generic testing process step for electronics packaging qualification and verification (PQV) including BGAs/DSBAs assemblies with consideration of heritage and heritage applicability. For all designs that are identified as requiring qualification by test, a test will be planned and implemented by the Lead Engineer with support of packaging reliability engineering as shown in the following subsections:

- A test plan is prepared by the Lead Engineer with support and approved by the PQV team.
- Flight-like hardware and test coupons should be built using flight processes.
- An approved PQV test facility should be identified.
- A Facility Survey of the test laboratory is conducted.
- An ESD survey of the test facilities is conducted if the hardware is ESD sensitive.
- An Operational Safety Survey of the test facilities and test set-up is conducted.
- A test procedure is prepared by the Lead Engineer with guidance from the PQV team for test parameters including failure definition; approved by PQV lead.
- A document with process steps defined in details is prepared by the Lead Engineer. Document also defines what criteria constitutes an anomaly and what is a failure.
- A review is conducted to ensure test readiness including the Lead Eng., Test Lead, Environmental Engineer, QA, Hardware Project Lead, PQV Team.
- A test dry run should be performed prior to the PQV test to optimize the test parameters of the chamber and meet the test requirements.
- Fail-safe settings for the temperature limits on the chamber are set to protect the hardware in the event of a malfunction or thermal run away.
- Pre-test functional tests of the unit under test (UUT) are performed and recorded. Data recording frequency should be determined between Lead Engineer and test house to catch any anomalies.

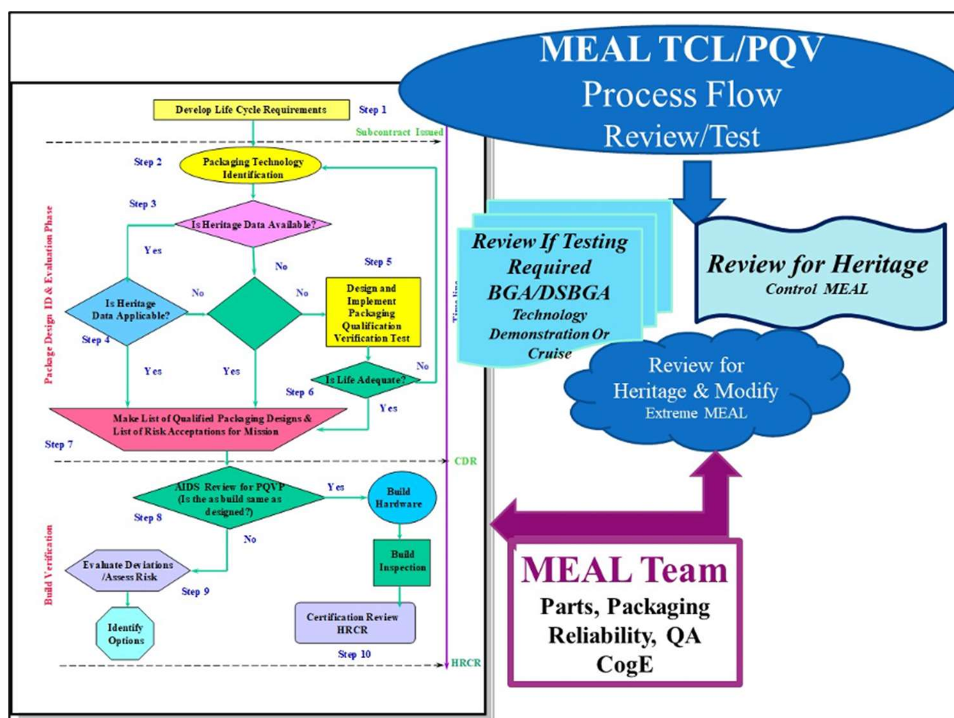

Figure 6-4. Generic testing process for electronics packaging qualification and verification (PQV) including BGAs/DSBAs Assemblies.

6.7 NON-TRADITIONAL TESTING: HALT/HASS FOR BGA/DSBGA

The previous testing methods were concentrated on piece-wise and bottom-up approach, which has been the qualification norm for the high-reliability industry. For COTS hardware including BGA/DSBA, however, a top level approach using HALT (Highly Accelerated Life Testing) to weed-out design weaknesses and to establish design margins is used. HALT is not MEAL, which does not intentionally induce failure and also considers end-of-mission conditions. HALT is used during design, and HASS (Highly Accelerated Stress Screening) for the flight hardware.

HASS may become a requirement for screening latent defect of high-density packaging and PCB either individually or at assembly level. For PCB microvia latent failure, IPC recently issued a warning. In a number of examples in high-profile hardware failures were not observed until after bare PCB fabrication, inspection, and acceptance. Many of these failures occurred within products that had already passed traditional production lot acceptance testing in accordance with existing IPC-6010, Printed Board Qualification and Performance Specifications. Data has been presented showing that traditional inspection techniques, using thermally stressed microsections and light microscopes alone is no longer an effective quality assurance tool for detecting failures of microvia-to-target plating. So, IPC is working on moving away from traditional microsection evaluations and focusing on performance-based acceptance testing using test coupons for acceptance to detect latent microvia failures.

7 SUMMARY

This guideline document presented recommendations for the use of COTS advanced plastic ball grid arrays (BGA) and die-size BGA (BGA) packaging technologies and assemblies for high-reliability and NASA spaceflight applications. It includes assembly and thermal cycle reliability test data for conventional and most advanced and high-density BGAs. These come in FCBGA configurations FCBGA with inputs/outputs (I/Os) as high as 1924 balls with 1 mm pitch and PBGA with 896 I/Os and 1 mm pitch as well as lower balls counts with pitches of 0.3 to 1.27 mm pitches. Evaluations included a 3D stack BGA with high lead tin-lead alloy solder balls. For the DSBGA assembly under thermal cycling, it used BGAs and LGA versions with 360 I/Os and 0.4 mm pitch for assembly conditioned with underfilling for comparison. DSBGAs had either tin-lead or lead-free (SAC) solder balls.

The guidelines presented cover the lessons learned from these two NEPP projects on BGAs and DSBGAs, as well as a literature search and lessons learned from spaceflight implementation of advanced electronics packaging technologies and COTS BGAs. For the two NEPP projects, it includes test results covering the key process issues, quality indicators, and quality assurance (QA) control parameters for assembly followed by comprehensive test data to address thermal cycle reliability and limitations at the assembly level. Finally, specific recommendations were given for low risk infusion spaceflight applications with consideration of MEAL requirements.

For MEAL identification, the Mission Types and risk postures are simplified to: (1) Low Risk Posture, Class A and B with moderate or extreme MEALs (short and/or long-time missions) and (2) Medium to high risk postures, Class D and Sub D with benign MEALs (short- and/or long-time missions). Key recommendations are the following:

- Narrow potential COTS packaging technologies and types using supplier data and application notes. Packaging technologies include: COTS high I/O flip-chip BGAs, low and high I/O wire-bond BGAs (gold/Cu with coating), and fine pitch DSBGAs. Review build up, materials, solder geometry and solder alloys (internal or external), heat distribution, etc.
- Review moisture sensitivity and bake out recommendations. Review non-standard PCB technologies for MEAL since a number of modifications are required to accommodate BGAs and especially DSBGAs. These include microvia and stacking, surface finish, and pad opening and mask.
- Follow manufacturer's recommendation for bake out preconditioning, assembly reflow profile, and underfill material for reliability optimization. Use daisy chain package as the test article for assembly verification and accelerated thermal cycle tests per industry standards. Include double-sided assembly if applicable.

Understanding current key COTS BGA/DSBGA packaging technologies with lessons learned is important in risk reduction for their use in high-reliability and spaceflight applications.

8 ACRONYMS AND ABBREVIATIONS

3D	multiple chips in three dimensional configuration
AC	acceleration cycling
ATC	acceleration thermal cycle
BGA	ball-grid array`
C4	controlled collapsible chip connector (at chip level)
C5	controlled collapsible chip connector connection (at package level)
COTS	commercial-off-the-shelf
CABGA	chip array ball grid array
CP-FC	copper pillar flip chip
CQFP	ceramic quad flat pack
CQFP	ceramic quad flat package
CSP	chip scale (size) package
CTBGA	thin core ball grid array
CTE	coefficient of thermal expansion
CTF	cycles to failure
CVBGA	very thin chip array ball grid array
DOE	design of experiment
DSBGA	die size ball grid array
EDX/EDS	energy dispersive X-ray/spectroscopy
EEE	electrical electronic and electromechanical
ENEPIG	electroless nickel electroless palladium and immersion gold
ESD	electro static discharge
eWLP	embedded wafer level package
eWLP-LGA	eWLP land grid array
FC	flip-chip

FCBGA	flip-chip ball grid array
FCV-BGA	very fine pitch flip-chip ball grid array
FOWLP	fan-out wafer level package
FPBGA	fine-pitch ball-grid array
FPGA	field programmable gate array
HALT	highly accelerated life test
HASL	hot air solder level
HASS	highly accelerated stress screening
HCI	hot carrier induced
I/O	input/output
IC	Integrated circuit
IMC	intermetallic compound
IPC	institute for interconnecting and packaging electronic circuits
IR	infrared
JPL	Jet Propulsion Laboratory
LGA	land grid array
MEAL	mission environment applications and lifetime
NASA	National Aeronautics and Space Administration
NBTI	negative biased temperature instability
NEPP	NASA Electronic Parts and Packaging
PBGA	plastic ball grid array
PCB	printed circuit board
PoP	package on package
PQV	packaging qualification and verification
QA	quality assurance
QFP	quad flat pack

QML	qualified manufacturer list
RDL	redistribution layer
RH	relative humidity
ROHS	restriction of hazardous substrate
SEM	scanning electron microscopy
SET	single event transient
SEU	single effect upset
SiP	system in package
SMC	surface mount component
SMT	surface mount technology
TC	thermal cycle
TDDB	time-dependent dielectric breakdown
Tg	glass transition temperature
TS	thermal shock
TSOP	thin small outline package
TV	test vehicle
VCE	vision compute element
ViP	via in pad
WB-BGA	wire-bond ball grid array
WLCSP	wafer level chip scale package
WLP	wafer-level package

9 REFERENCES

NASA-STD-8739.1, Workmanship Standard For Polymeric Application On Electronic Assemblies

J-STD-001xS Space Hardware Addendum: Space Applications Electronic Hardware Addendum for J-STD-001. The addendum MUST be used with the same version of the standard; e.g. 001CS with 001C, 001DS with 001D, 001ES with 001E

IPC-7094: Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7095: Design and Assembly Process Implementation for BGAs

IPC-9701: Qualification and Performance Test Methods for Surface Mount Solder Attachments

PC/JEDEC-9706: Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

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