

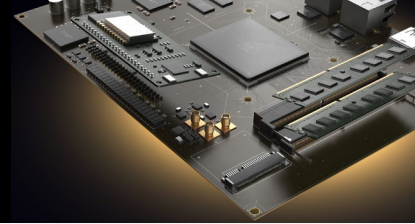


AltiumLive 2018 University Day

Instructor

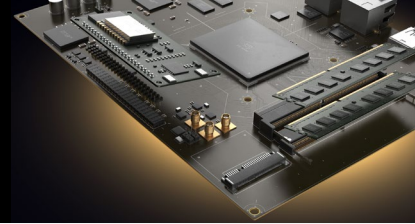
Derek Jackson CID+
Product Expert

Altium



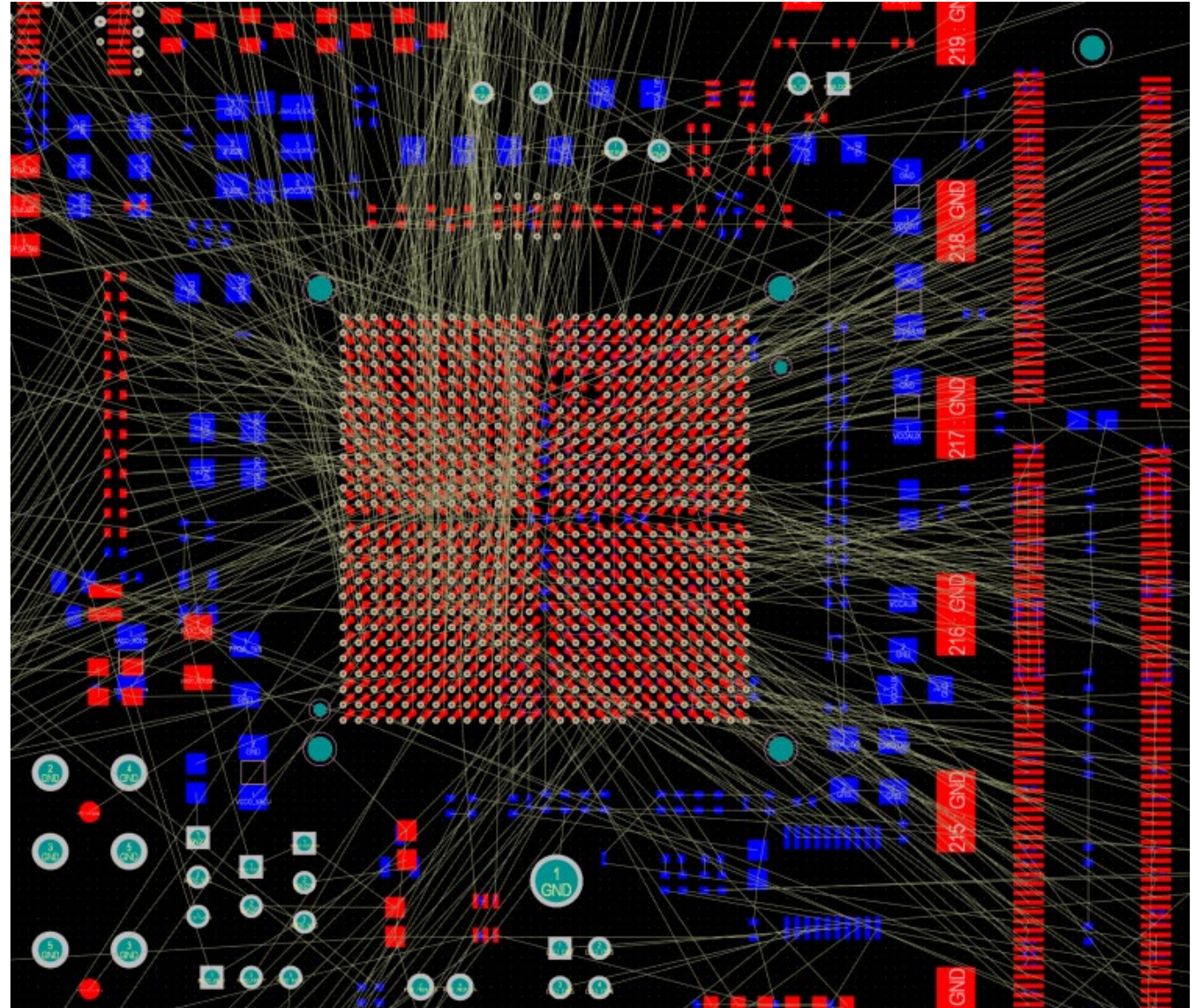
How to Route and tune high speed topologies with xSignals

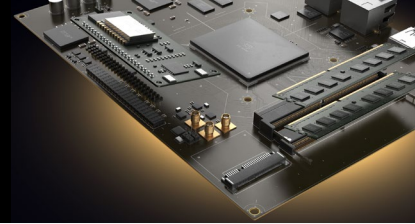
A look at xSignals in Altium Designer.



Nets (in review)

- Nets are assigned at the schematic level and transferred to the PCB.
- In the Pcb document, without any routing, we see connection lines between unconnected primitives of the same net.



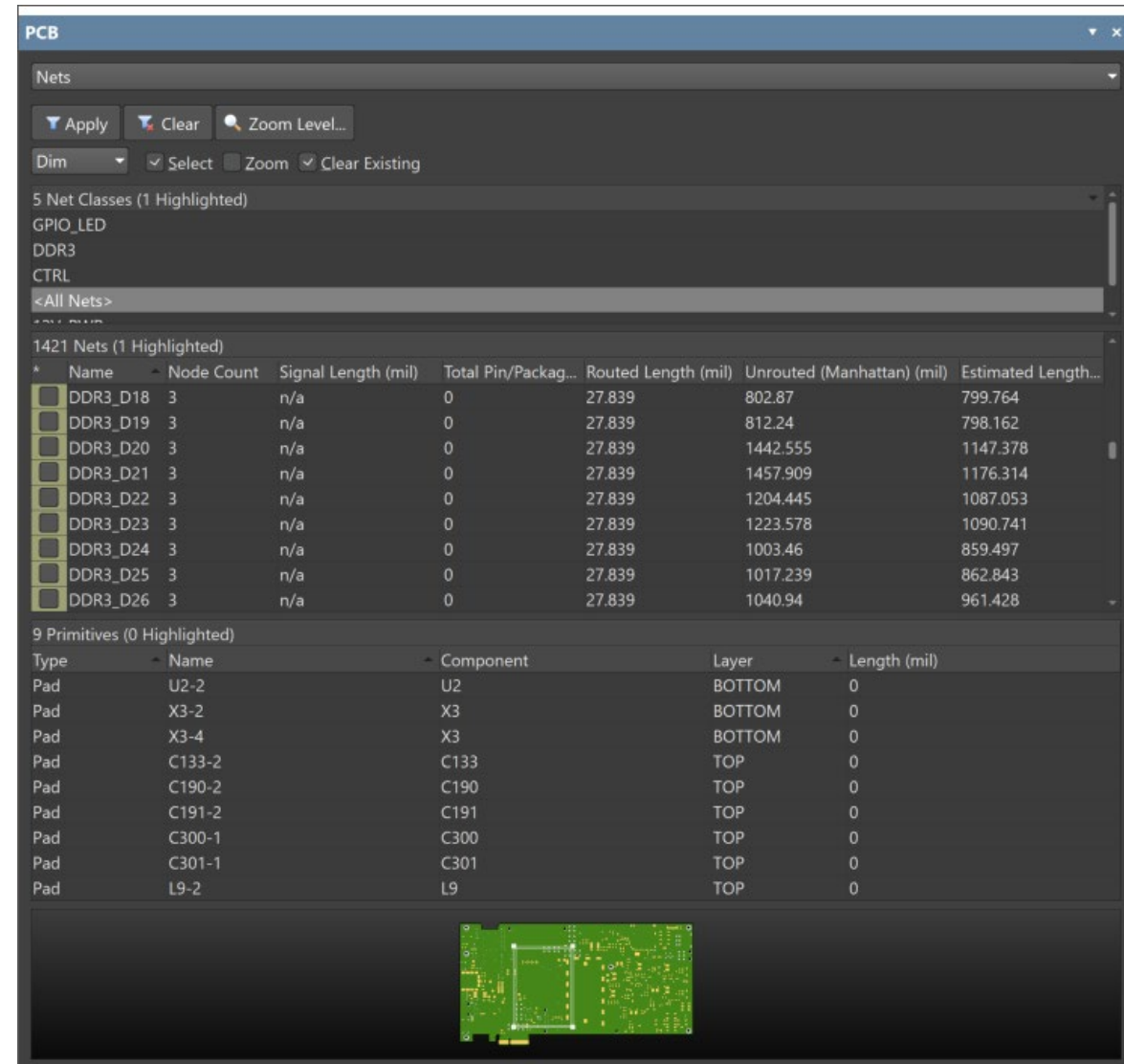


Nets (in review)

In the PCB Panel, under the Nets section, we can see net information , including:

- **Net Name**
- **Routed Net Length:** The routed track length that does not sort out overlapping segments.
- **Signal Length:** A calculated distance that provides an accurate calculation length of routing between two pad objects, excluding track overlaps in the total, and handles fills, via lengths.

For more than two connected nodes, this will display **n/a**.



PCB

Nets

Apply Clear Zoom Level...

Dim Select Zoom Clear Existing

5 Net Classes (1 Highlighted)

GPIO_LED
DDR3
CTRL

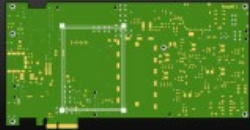
<All Nets>

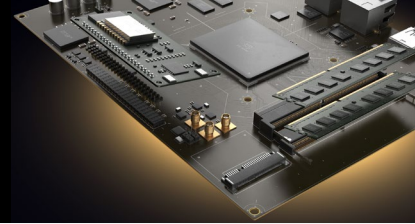
1421 Nets (1 Highlighted)

Name	Node Count	Signal Length (mil)	Total Pin/Packag...	Routed Length (mil)	Unrouted (Manhattan) (mil)	Estimated Length...
DDR3_D18	3	n/a	0	27.839	802.87	799.764
DDR3_D19	3	n/a	0	27.839	812.24	798.162
DDR3_D20	3	n/a	0	27.839	1442.555	1147.378
DDR3_D21	3	n/a	0	27.839	1457.909	1176.314
DDR3_D22	3	n/a	0	27.839	1204.445	1087.053
DDR3_D23	3	n/a	0	27.839	1223.578	1090.741
DDR3_D24	3	n/a	0	27.839	1003.46	859.497
DDR3_D25	3	n/a	0	27.839	1017.239	862.843
DDR3_D26	3	n/a	0	27.839	1040.94	961.428

9 Primitives (0 Highlighted)

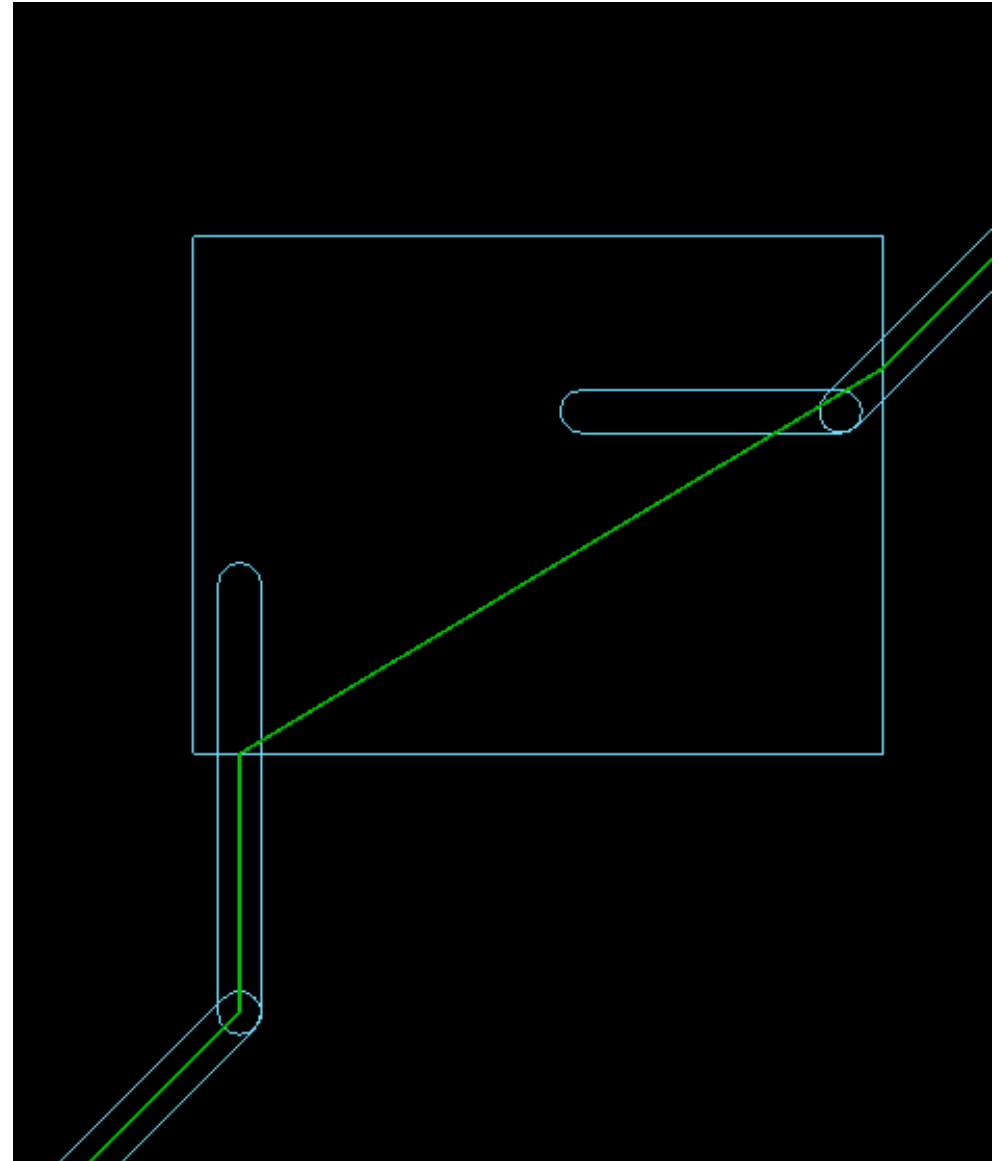
Type	Name	Component	Layer	Length (mil)
Pad	U2-2	U2	BOTTOM	0
Pad	X3-2	X3	BOTTOM	0
Pad	X3-4	X3	BOTTOM	0
Pad	C133-2	C133	TOP	0
Pad	C190-2	C190	TOP	0
Pad	C191-2	C191	TOP	0
Pad	C300-1	C300	TOP	0
Pad	C301-1	C301	TOP	0
Pad	L9-2	L9	TOP	0

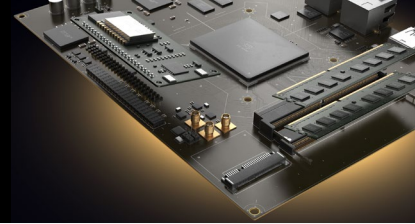




Nets (in review)

- **Signal Length:** The Signal length is automatically generated, and we have no control over it. Well are going to learn how to setup our own “Accurate” length using xSignals in this discussion.
- **More info:** You can read more about Nets in the PCB here:
[https://www.altium.com/documentation/18.1/display/ADES/PCB_Pnl-PCB\(\(PCB+--+Nets\)\)_AD](https://www.altium.com/documentation/18.1/display/ADES/PCB_Pnl-PCB((PCB+--+Nets))_AD)



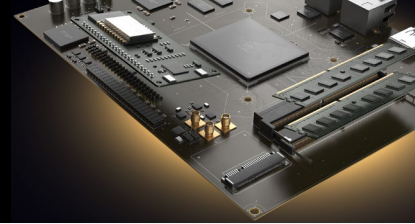


Length Tuning:

- For signals that need to travel from a source component and arrive at different destinations at the same time will need to have their routed tracks the same length. This is done using various Length Matching techniques.

- **More info:**

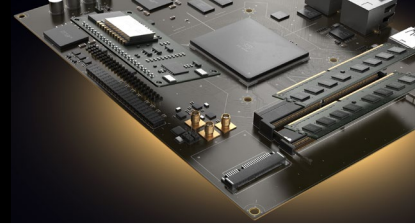
[https://www.altium.com/documentation/18.1/display/ADES/\(\(Length+Tuning\)\)
AD](https://www.altium.com/documentation/18.1/display/ADES/((Length+Tuning))_AD)



Length Matching Rules

Length Matching Rule:

- In Altium Designer, a Matched Length Rule can be defined which defines the allowable range of the track lengths (**Design » Rules » High Speed » Matched Lengths**) for the specified nets.



Length Matching Rules

The rule interprets lengths from all the routed nets referenced by the rule as follows:

Matched Net Length's **Min Limit** = Longest Net – Rule Tolerance

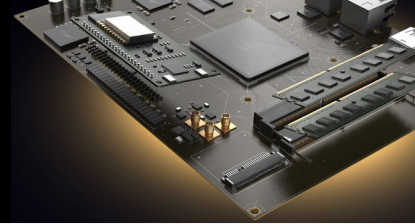
Matched Net Length's **Max Limit** = Longest Net

(constrained by the *length rule*)

Valid Range = Highest Min Limit to Lowest Max Limit

(most stringent combination of Length and Matched Length rules)

Target Length = Lowest **Max Limit**



Matched Length Rule:

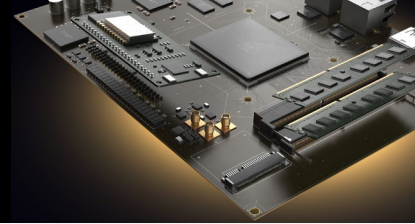
“Group Matched Lengths”: Set the target for all nets targeted by the rule, looking at the longest net length to set the maximum.

“Within Differential Pair Length”: Matched length is between the legs of a differential pair.

Tolerance: Provides the amount of variance from the total routed length by up to this amount. The target length range is defined by the equation:

$$\text{(Longest Length - Tolerance)} \leq \text{Current Length} \leq \text{Longest Length}$$

[https://www.altium.com/documentation/18.1/display/ADES/PCB_Dlg-MatchedNetLengthsRule_Frame\(\(Matched+Lengths\)\)_AD](https://www.altium.com/documentation/18.1/display/ADES/PCB_Dlg-MatchedNetLengthsRule_Frame((Matched+Lengths))_AD)



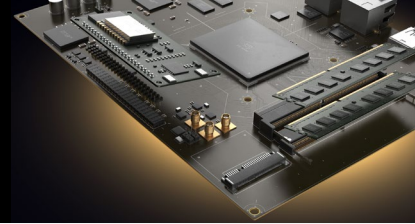
Interactive Length Tuning

- When length tuning (**Route » Interactive Length Tuning**), selecting a track to tune, a length gage is displayed showing the Min/Max Length, estimated length, and the target length.

Pressing the Tab key, the **Min** and **Max** Limits will be displayed in the Properties panel.

In the PCB Panel (Nets section) the net length is color coded for easy viewing.

- **No highlight** color = length is within tolerance.
- **Yellow** highlight color = the route length is less than the rule minimum.
- **Red** highlight color = the route length is greater than the rule maximum.



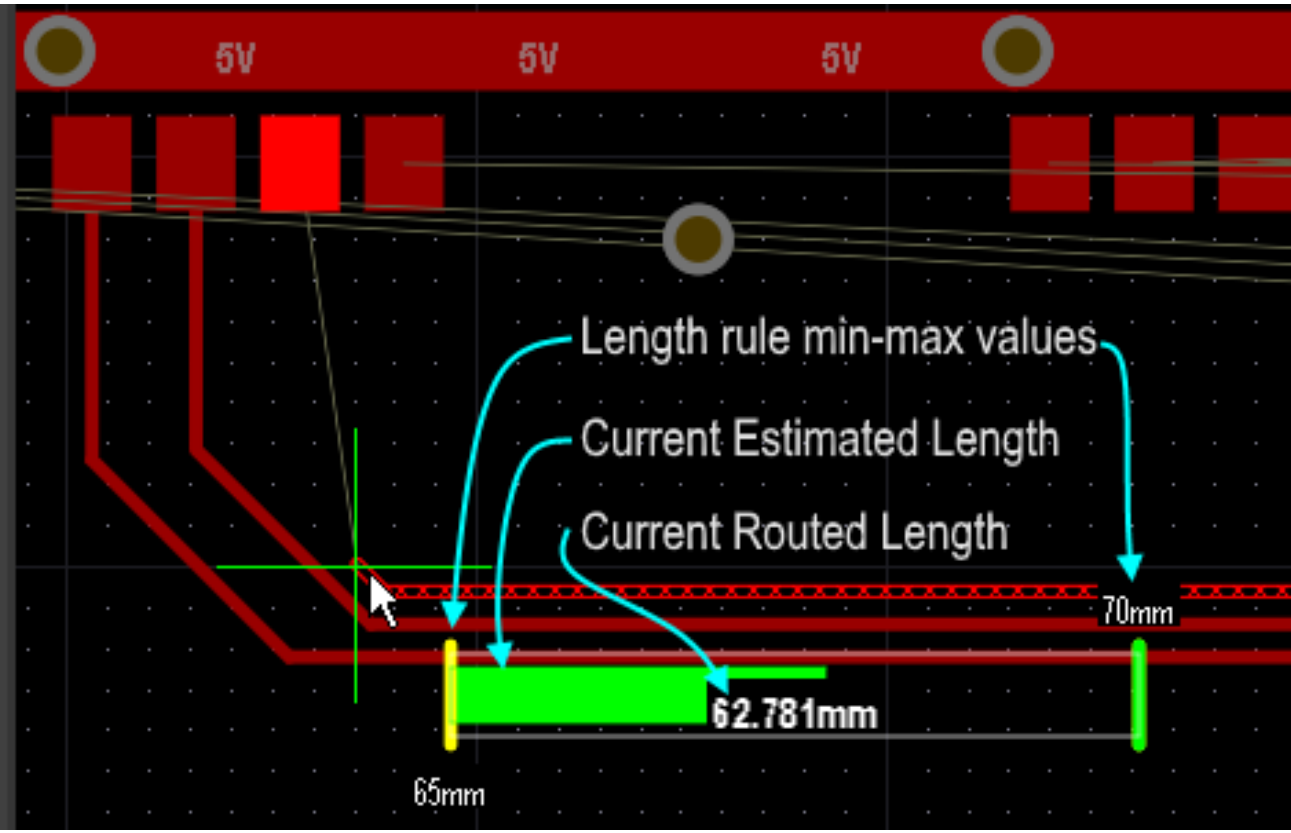
Interactive Length Tuning

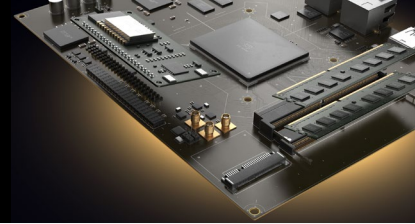
8 Nets (1 Highlighted)

* Name	Routed Le...	Estimated L...	Signal Length (Unrouted (Ma...
LCD_DB0	70.207	70.207	70.207	0
LCD_DB1	68.944	68.944	68.944	0
LCD_DB2	62.781	67.723	n/a	5.59
LCD_DB3	0	60.45	61.245	61.245
LCD_DB4	0	52.556	52.855	52.855
LCD_DB5	0	51.313	52.985	52.985
LCD_DB6	0	50.063	52.215	52.215
LCD_DB7	0	48.82	51.445	51.445

4 Primitives (0 Highlighted)

Type	Name	Component	Layer	Length (mm)
Pad	RA2-7	RA2	Top Layer 0	
Pad	U1-17	U1	Top Layer 0	
Track	Width=0.2mm (190		Top Layer 5.551	
Track	Width=0.2mm (193		Top Layer 5.556	

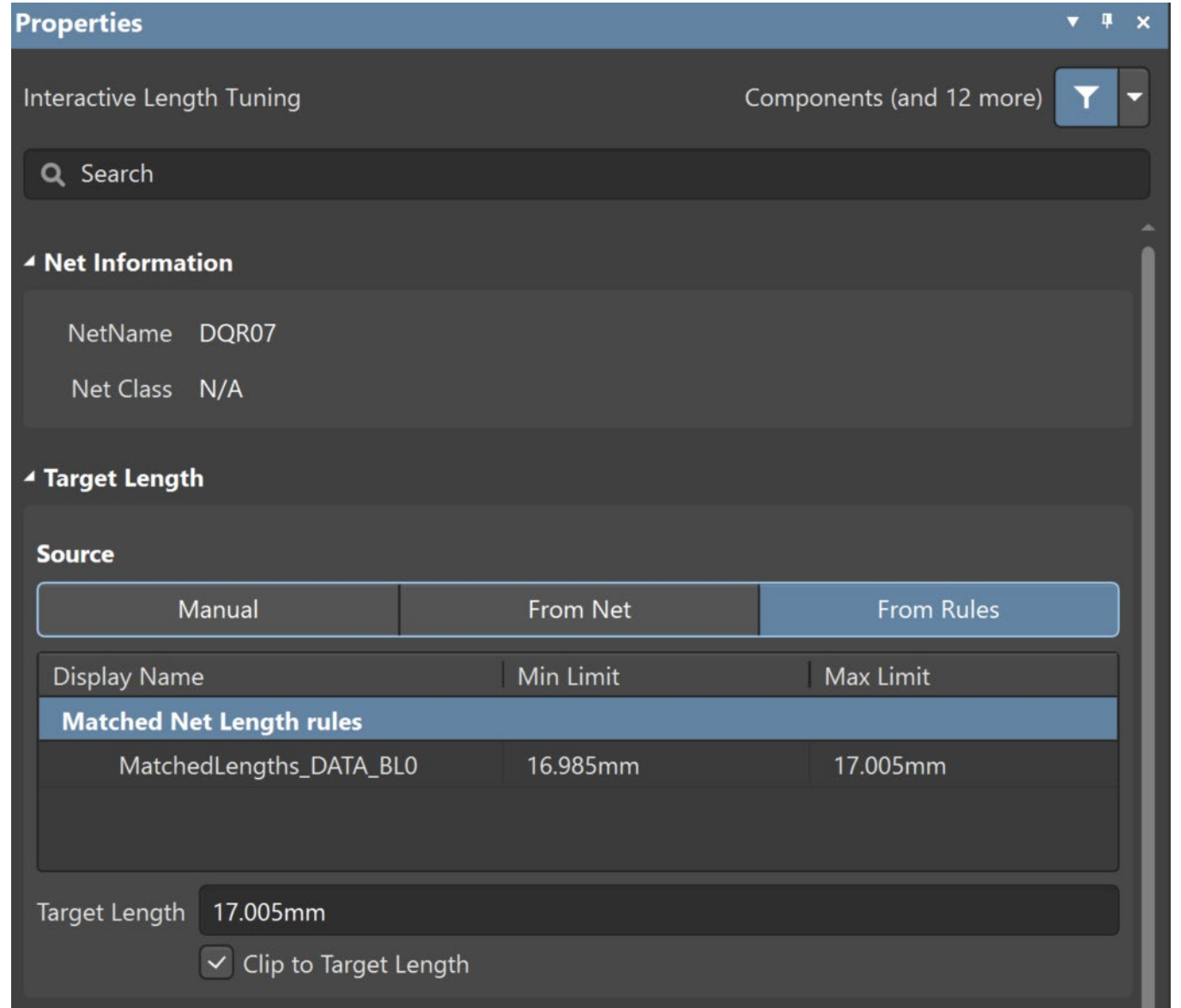




Interactive Length Tuning

There are three ways to define the length limits when tuning:

- Manual
- From Net
- From Rules

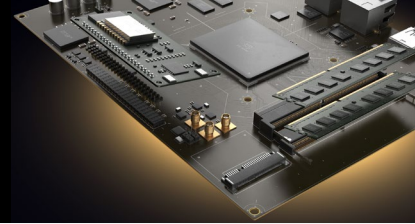


The screenshot shows the 'Properties' window for 'Interactive Length Tuning'. It includes a search bar, a filter for 'Components (and 12 more)', and two expandable sections: 'Net Information' and 'Target Length'. The 'Target Length' section has three tabs: 'Manual', 'From Net', and 'From Rules', with 'From Rules' selected. Below the tabs is a table of 'Matched Net Length rules' with columns for 'Display Name', 'Min Limit', and 'Max Limit'. At the bottom, there is a 'Target Length' input field set to '17.005mm' and a checked checkbox for 'Clip to Target Length'.

Display Name	Min Limit	Max Limit
Matched Net Length rules		
MatchedLengths_DATA_BLO	16.985mm	17.005mm

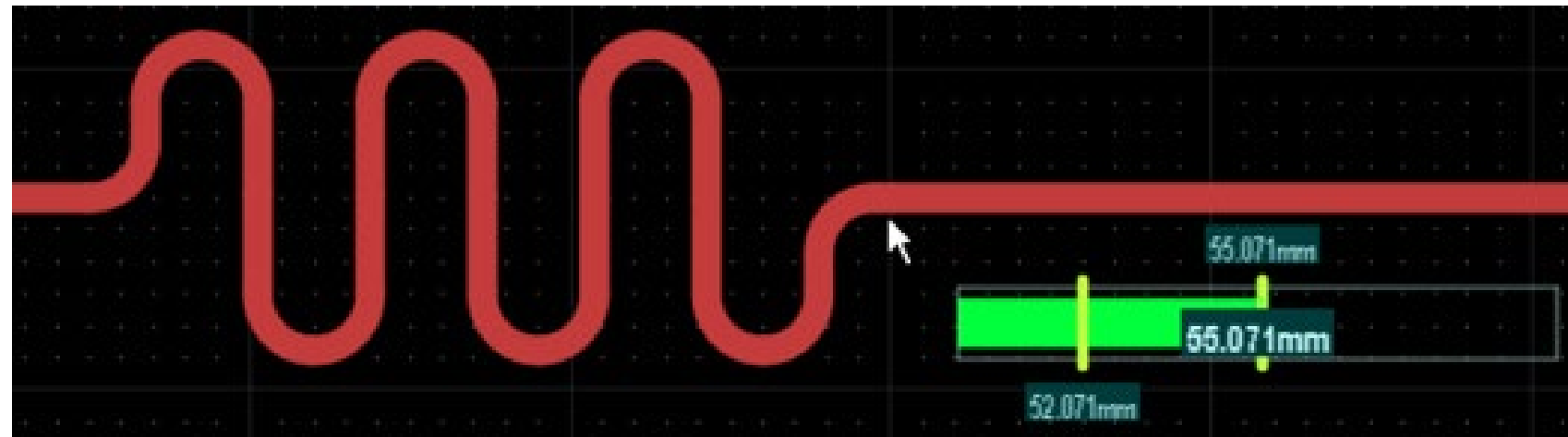
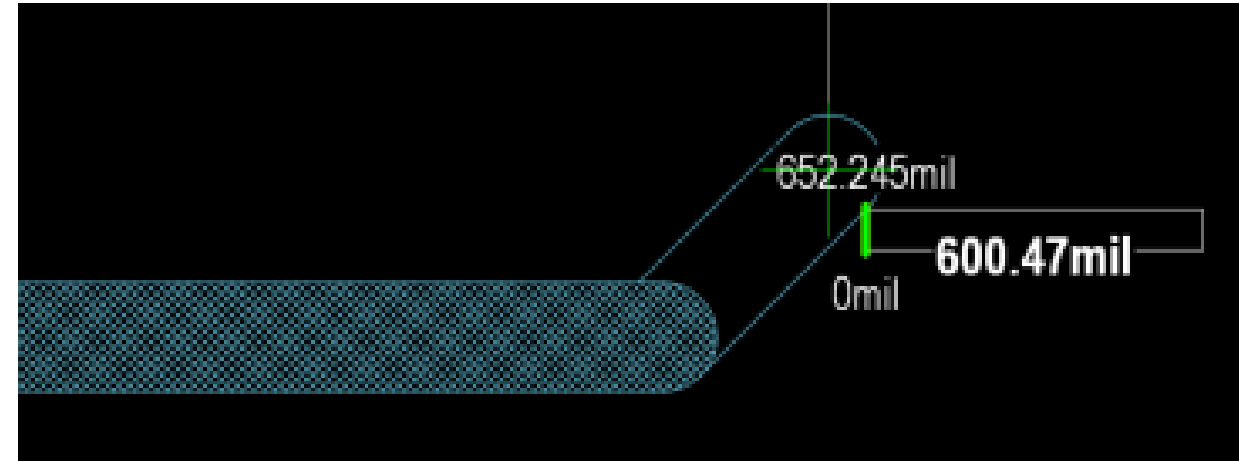
Target Length: 17.005mm

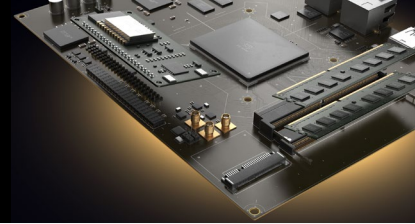
Clip to Target Length



Interactive Length Tuning

- During routing, display the length gage by pressing **Shift+G**
- If no Length Matching rule applies, the min/max will display 0/Current length or 0/0.
- During Length Tuning, the Min, Max, and target lengths are shown.

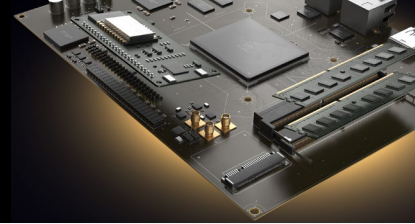




Accordions:

For length tuning, accordions are the length of track added to the route to increase the length.

- Style: Mitered Lines/Arcs or Rounded. (**Space Bar** to cycle)
- Interactive Routing: When routing, accordions can be added by pressing **Shift+A**.
- Tab: pressing Tab during a tuning / Routing command, will display its properties in the Pattern section, allowing adjustments. amplitude, gap, and miter. Shortcuts are listed in the Panel. During the command, you can press the ~ to get a list of shortcuts.



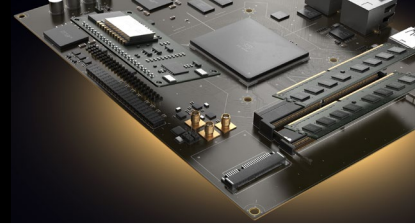
Accordion Object:

For length tuned tracks, an accordion control object gets added with the length tuning. Its control appears as a bounding box around the tuned section. Modifying an accordion:

- Double-clicking: Select an accordion to edit its properties in the Properties Panel.
- Dragging: Dragging the sides or vertices of the accordion object will adjust the added tuning and scale accordingly.

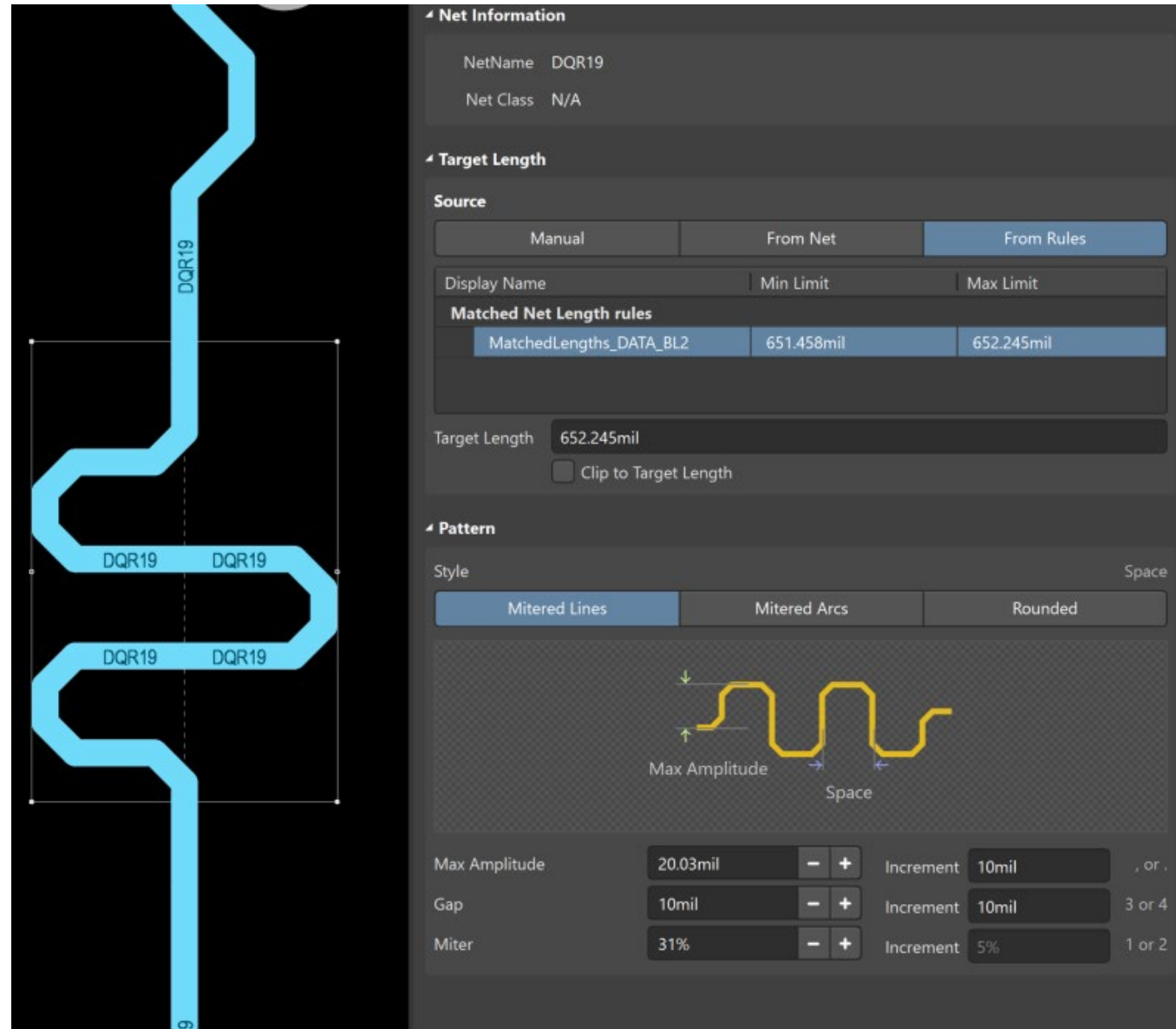
*Currently, accordion control objects are not added when tuning Differential Pairs:
(<https://bugcrunch.live.altium.com/#Idea/8016>)*

More Info: [https://www.altium.com/documentation/18.1/display/ADES/PCB_Obj-Accordion\(\(Accordion\)\)_AD](https://www.altium.com/documentation/18.1/display/ADES/PCB_Obj-Accordion((Accordion))_AD)



Accordion Object:

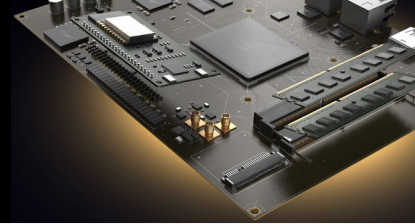
Shown selected with properties showing in Properties Panel.



The screenshot displays a net named 'DQR19' in a light blue color, selected with a white border. The net is routed in a complex, zig-zag pattern. The Properties Panel on the right shows the following settings:

- Net Information**
 - NetName: DQR19
 - Net Class: N/A
- Target Length**
 - Source: From Rules (selected)
 - Matched Net Length rules:

Display Name	Min Limit	Max Limit
MatchedLengths_DATA_BL2	651.458mil	652.245mil
 - Target Length: 652.245mil
 - Clip to Target Length
- Pattern**
 - Style: Mitered Lines (selected), Mitered Arcs, Rounded
 - Space: (indicated by a double-headed arrow in the diagram)
 - Max Amplitude: 20.03mil (with - and + buttons)
 - Increment: 10mil (with , or . separator)
 - Gap: 10mil (with - and + buttons)
 - Increment: 10mil (with 3 or 4 separator)
 - Miter: 31% (with - and + buttons)
 - Increment: 5% (with 1 or 2 separator)



Accordions:

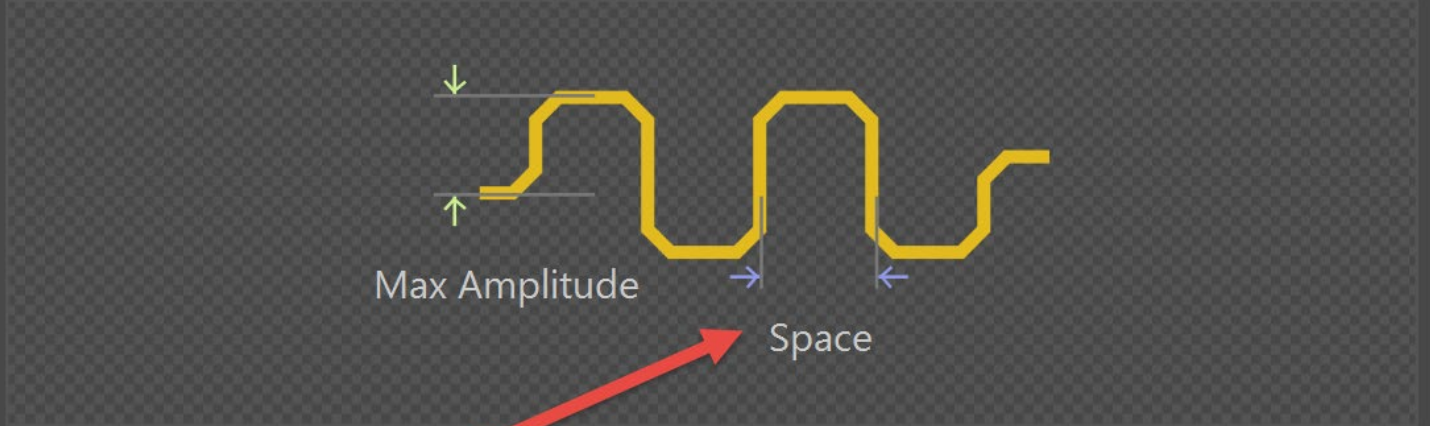
The Accordion style can be 90, mitered with lines or serpentine.

- When using miters, the Space is the inner gap, and the miter is represented as a percentage of the space length value.

Pattern

Style Space

Mitered Lines Mitered Arcs Rounded



Max Amplitude Space

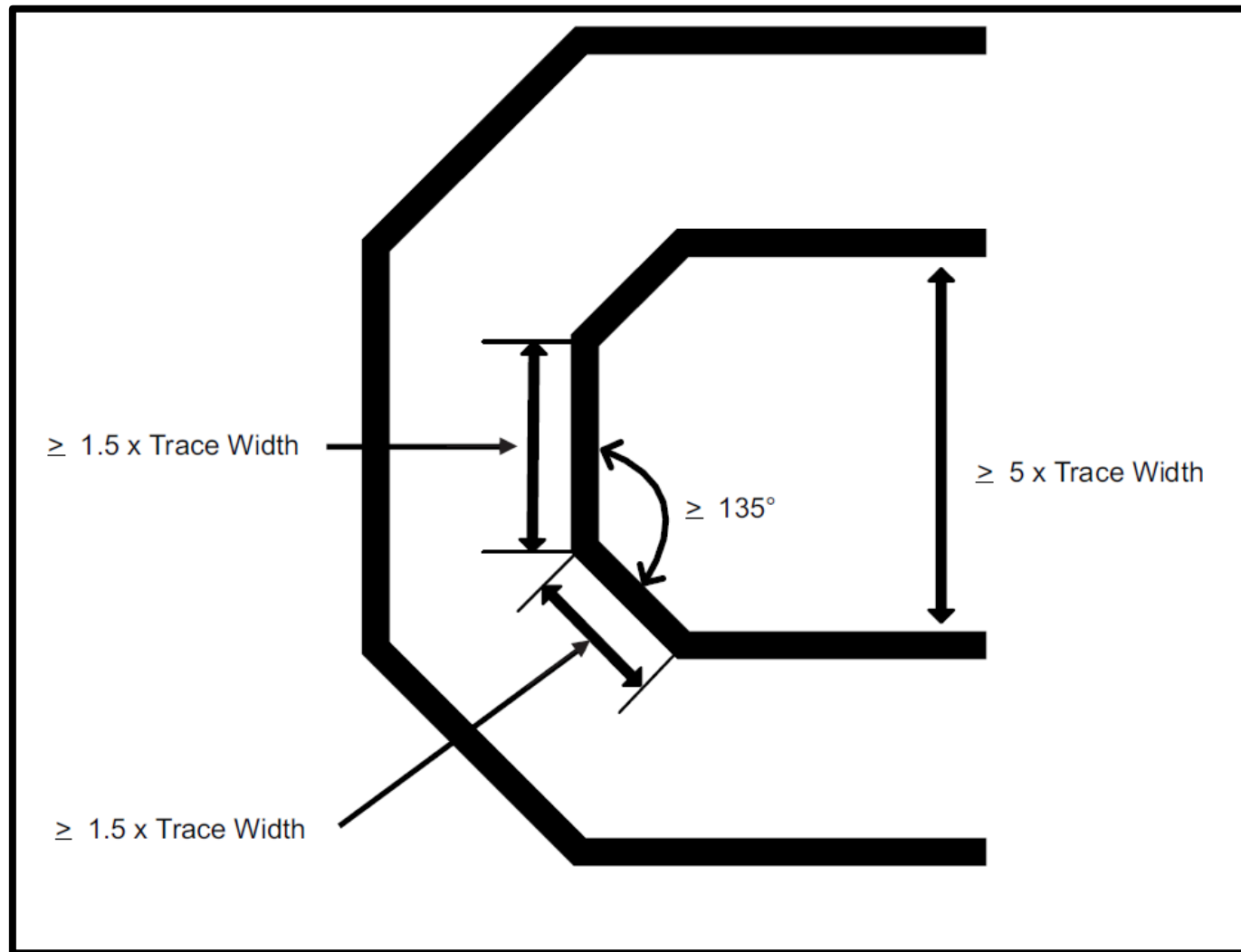
Max Amplitude	3.748mm	-	+	Increment	0.05mm	, or .
Space	0.3mm	-	+	Increment	0.05mm	3 or 4
Miter	25%	-	+	Increment	5%	1 or 2



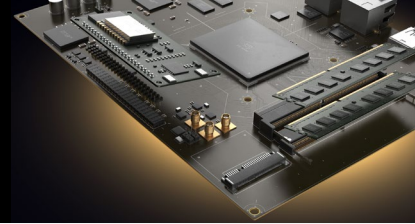
Accordions:

So, what value do you use for the miter percentage?

- Typically Space = 3-5 x Width, Miter $\geq 1.5 \times W$ and Top line is $1.5 \times W$.
- The Texas Instrument's [USB3 guide](#) recommends that the space is 5x the width, the length of the inner bend is $1.5 \times$ the trace width, and the inner segment's top of the bend is $1.5 \times$ as shown.



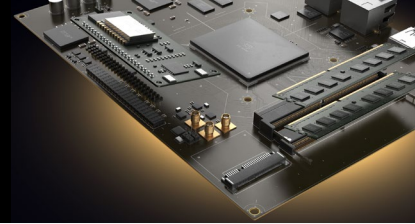
- [Extra reading: https://docs.toradex.com/102492-layout-design-guide.pdf](https://docs.toradex.com/102492-layout-design-guide.pdf)



xSignals:

An xSignal is defined as a path for a signal to travel between a source and destination (pin pairs), and can include termination components as well as branches (Balanced-T or Fly-By).

- Virtual Net: Similar to the Signal Length calculation, but differs that xSignals can be created and used for accurate route measurements.
- Creation: xSignals can be created with or without routing between the selected pin pairs.
 - xSignals can be created from selected Pads, components or the xSignal wizard.
 - xSignals will follow the routing topology set for the selected nets.



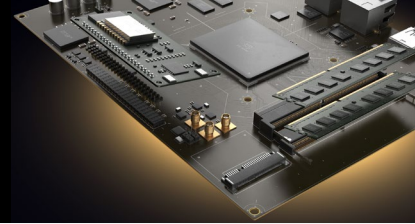
xSignal Creation:

Accessing the **xSignals** menu (**Design » xSignals**), depending on what is selected will affect available menu options...

- From the Menu:
 - » **Run xSignals Wizard**
 - » **Create xSignals**
- With Pads selected (from menu or right-clicking on a selected pad):
 - » **Create xSignal from selected pins**
- With Components selected:
 - » **Create xSignals between components**
 - » **Create xSignals from connected Nets**

More information:

[https://www.altium.com/documentation/18.1/display/ADES/\(\(Defining+High+Speed+Signal+Paths+with+xSignals\)\)](https://www.altium.com/documentation/18.1/display/ADES/((Defining+High+Speed+Signal+Paths+with+xSignals))) AD



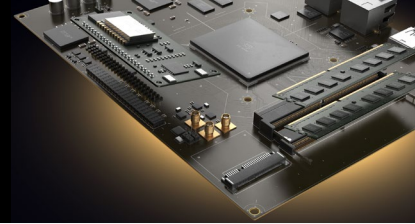
xSignal Panel:

There are three regions in the xSignal section of the PCB panel:

- xSignal Classes
- xSignals belonging to the selected class
- Primitives in the xSignal (pads, tracks, arcs, and vias)

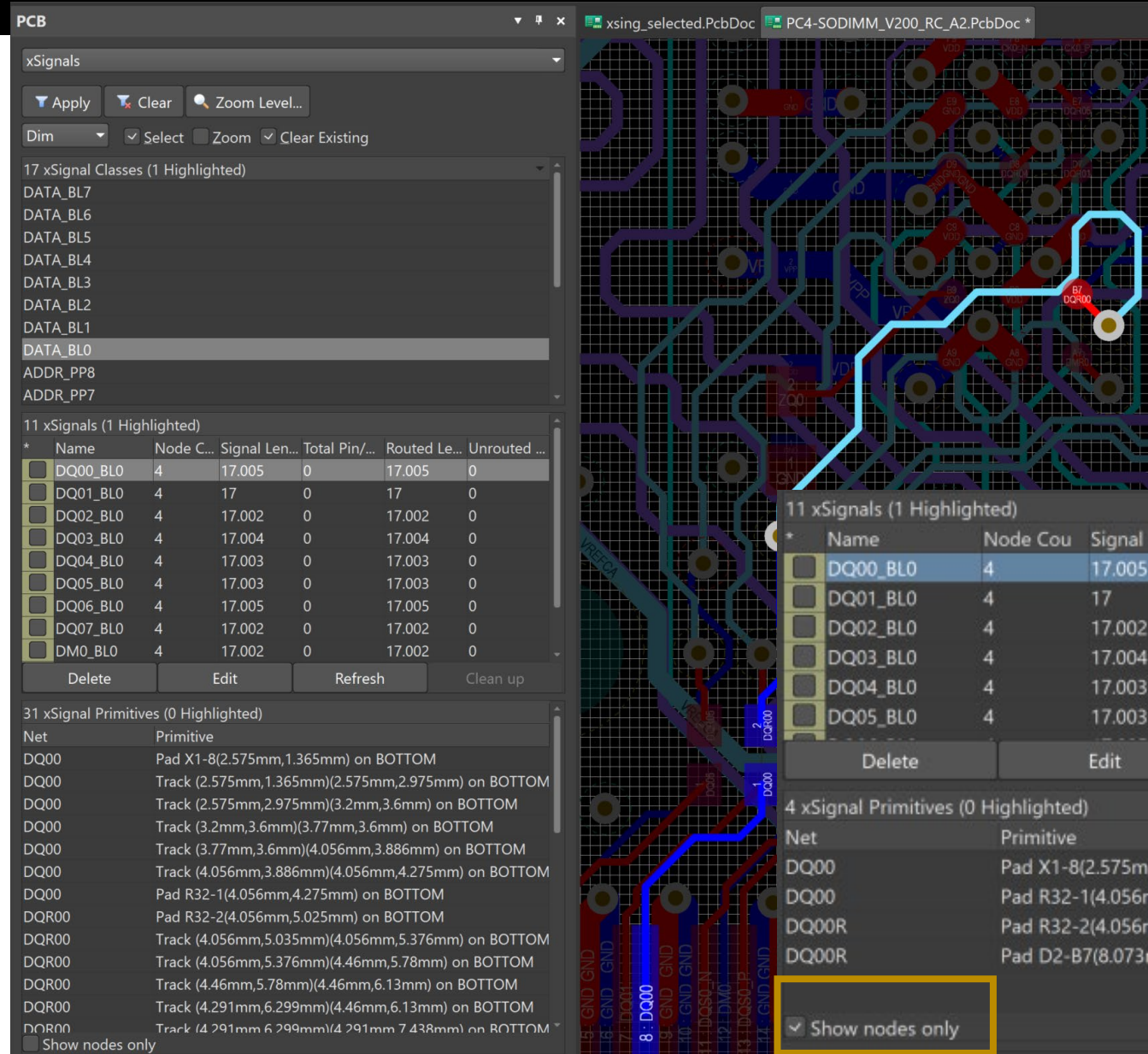
In the xSignal section of the PCB panel, we also see Signal Length, Routed Length, Unrouted Length, and Total Pin/Package length.

Similarly to the Nets section, for Length Matching rules we will see the nets lengths change color based if they are **shorter**, **longer**, or in the target length range as we saw earlier.



xSignal Panel:

Shown, for the selected Net signal, all primitives are shown. Clicking the Show nodes only will only display connected Pads.



xSignals

Apply Clear Zoom Level...

Dim Select Zoom Clear Existing

17 xSignal Classes (1 Highlighted)

- DATA_BL7
- DATA_BL6
- DATA_BL5
- DATA_BL4
- DATA_BL3
- DATA_BL2
- DATA_BL1
- DATA_BL0
- ADDR_PP8
- ADDR_PP7

11 xSignals (1 Highlighted)

Name	Node C...	Signal Len...	Total Pin/...	Routed Le...	Unrouted ...
DQ00_BL0	4	17.005	0	17.005	0
DQ01_BL0	4	17	0	17	0
DQ02_BL0	4	17.002	0	17.002	0
DQ03_BL0	4	17.004	0	17.004	0
DQ04_BL0	4	17.003	0	17.003	0
DQ05_BL0	4	17.003	0	17.003	0
DQ06_BL0	4	17.005	0	17.005	0
DQ07_BL0	4	17.002	0	17.002	0
DM0_BL0	4	17.002	0	17.002	0

Delete Edit Refresh Clean up

31 xSignal Primitives (0 Highlighted)

Net	Primitive
DQ00	Pad X1-8(2.575mm,1.365mm) on BOTTOM
DQ00	Track (2.575mm,1.365mm)(2.575mm,2.975mm) on BOTTOM
DQ00	Track (2.575mm,2.975mm)(3.2mm,3.6mm) on BOTTOM
DQ00	Track (3.2mm,3.6mm)(3.77mm,3.6mm) on BOTTOM
DQ00	Track (3.77mm,3.6mm)(4.056mm,3.886mm) on BOTTOM
DQ00	Track (4.056mm,3.886mm)(4.056mm,4.275mm) on BOTTOM
DQ00	Pad R32-1(4.056mm,4.275mm) on BOTTOM
DQR00	Pad R32-2(4.056mm,5.025mm) on BOTTOM
DQR00	Track (4.056mm,5.035mm)(4.056mm,5.376mm) on BOTTOM
DQR00	Track (4.056mm,5.376mm)(4.46mm,5.78mm) on BOTTOM
DQR00	Track (4.46mm,5.78mm)(4.46mm,6.13mm) on BOTTOM
DQR00	Track (4.291mm,6.299mm)(4.46mm,6.13mm) on BOTTOM
DQR00	Track (4.291mm,6.299mm)(4.291mm,7.438mm) on BOTTOM

Show nodes only

11 xSignals (1 Highlighted)

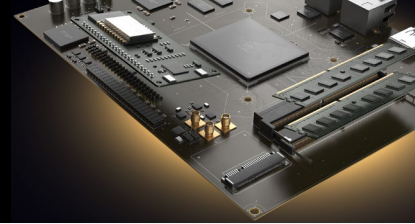
Name	Node Cou	Signal Lengt...	Total Pin/Pac...	Routed Lengt...	Unrouted (M...
DQ00_BL0	4	17.005	0	17.005	0
DQ01_BL0	4	17	0	17	0
DQ02_BL0	4	17.002	0	17.002	0
DQ03_BL0	4	17.004	0	17.004	0
DQ04_BL0	4	17.003	0	17.003	0
DQ05_BL0	4	17.003	0	17.003	0

Delete Edit Refresh Clean up

4 xSignal Primitives (0 Highlighted)

Net	Primitive
DQ00	Pad X1-8(2.575mm,1.365mm) on BOTTOM
DQ00	Pad R32-1(4.056mm,4.275mm) on BOTTOM
DQ00R	Pad R32-2(4.056mm,5.025mm) on BOTTOM
DQ00R	Pad D2-B7(8.073mm,10.517mm) on TOP

Show nodes only

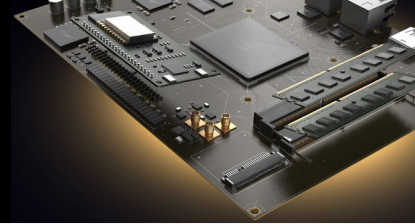


Pin-Package Delays:

- To account for the length added from routing inside the chip package, most manufacturers will supply a pin package length.
- Adding a pin package length to your footprint will add the total package length to the calculated signal length when a single track connects to it (flyby topologies are excluded).
- The length can be define at the schematic level (recommended), or directly in the PCB.
- [The Intel Memory Interface Handbook](#) recommends including package delays for speeds greater than 800MHz.

Extra reading Pin Pairs:

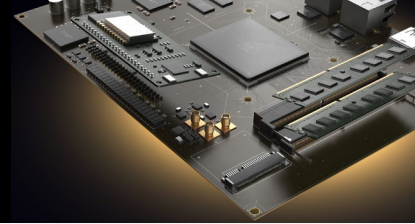
[https://www.altium.com/documentation/18.0/display/ADES/PCB_Cmd-ManagePinPairs\(\(ManagePinPairs\)\)_AD](https://www.altium.com/documentation/18.0/display/ADES/PCB_Cmd-ManagePinPairs((ManagePinPairs))_AD)



xSignal Wizard:

The intent of this wizard is to automatically create the xSignals, Matched Length Groups, Diff Pair Matched Lengths.

- xSignals Wizard: allows creating:
 - **DDR3/4**
 - **USB 3.0**
 - **Custom Multi-Component Interconnect**



xSignal Wizard:

DDR3

- Supports Flyby or Balanced T.
- For Balanced T topology, at the separation point, signals must use a special single pad component to define the split point.
- Do not use # in net names as this represents the bank number when defining.

xSignal Multi-Chip Wizard [mm] ✕

Select the Circuit
Choose a circuit type or use Custom for general multi-component xSignals

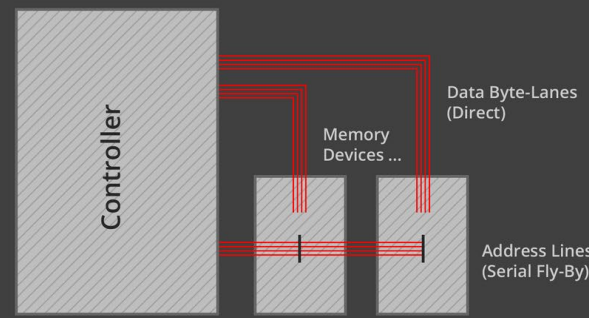
On-Board DDR3 / DDR4

USB 3.0

Custom Multi-Component Interconnect

Selected Circuit

DDR3/4



Data Bus Width (# of Data Lines in each Byte-Lane)

Address/Cmd/Ctrl Match Length Tolerance

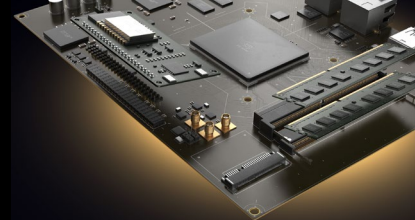
Data Byte-Lanes Matched Length Tolerance

Clock Within Diff Pair Length Tolerance

Notes:

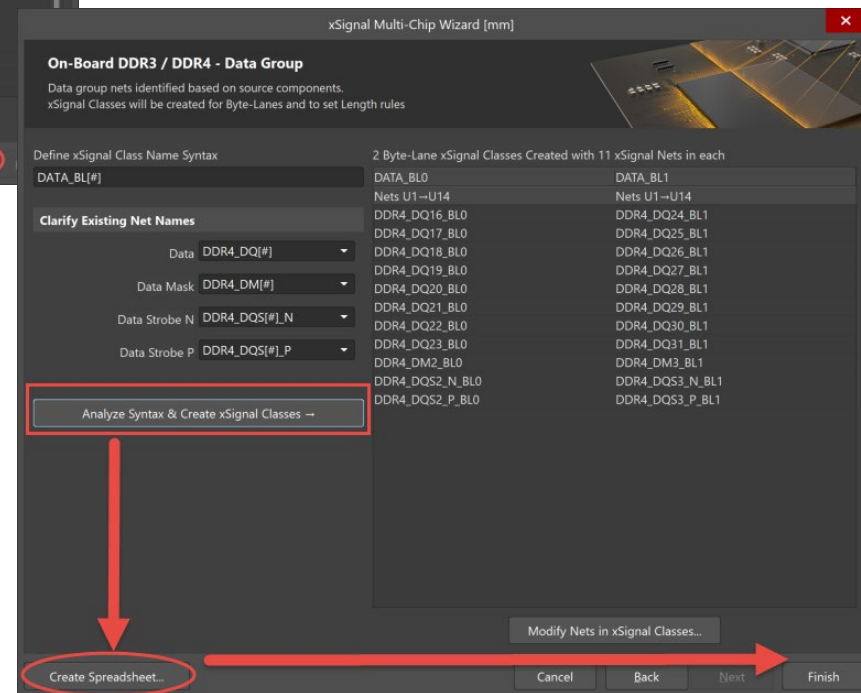
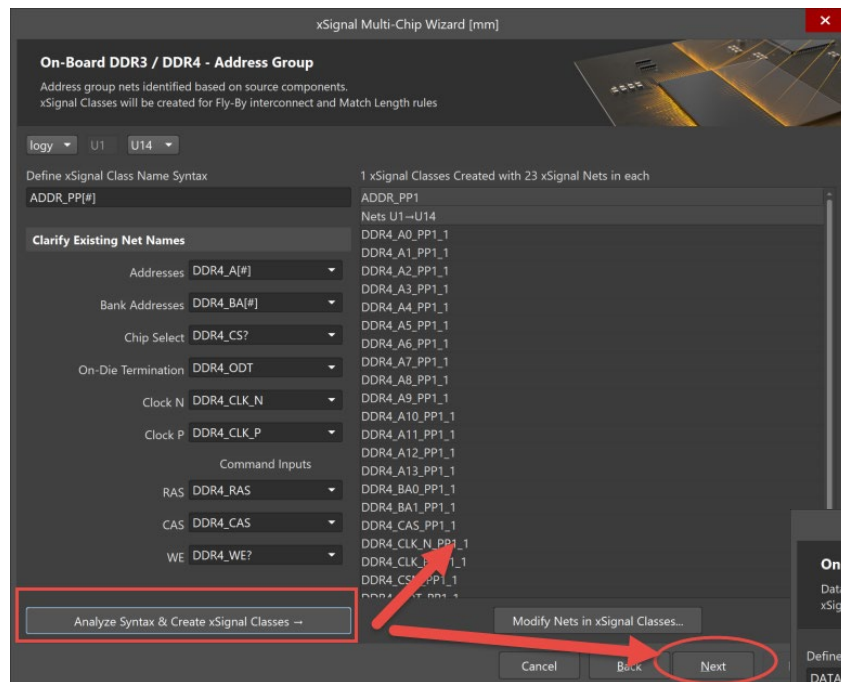
1. Address Group: A Matched Length rule set will be created for each Fly-By set from the Address, Command and Control signals. Multiple clocks will be accommodated.
2. Data Group: Multiple Byte-Lane Matched Length rule sets created based on the Data Bus Width.
3. If the Clock is to be routed longer than the Matched set to center the eye on the sample, then after routing and tuning the Matched set, lengthen the clock as described in data sheet.
4. Pin-Package lengths will be included for the source and target pins in the length calculations.

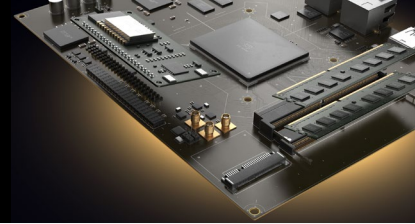
Cancel
Back
Next
Finish



DDR3

- Click the Analyze button once net names are filled in.
- Use # to represent the banks.
- Use * and ? Wildcards when necessary.
- Click the Modify Nets to add/remove nets as required.
- On Data source page, click the Create Datasheet to get detailed output of generated xSignals.

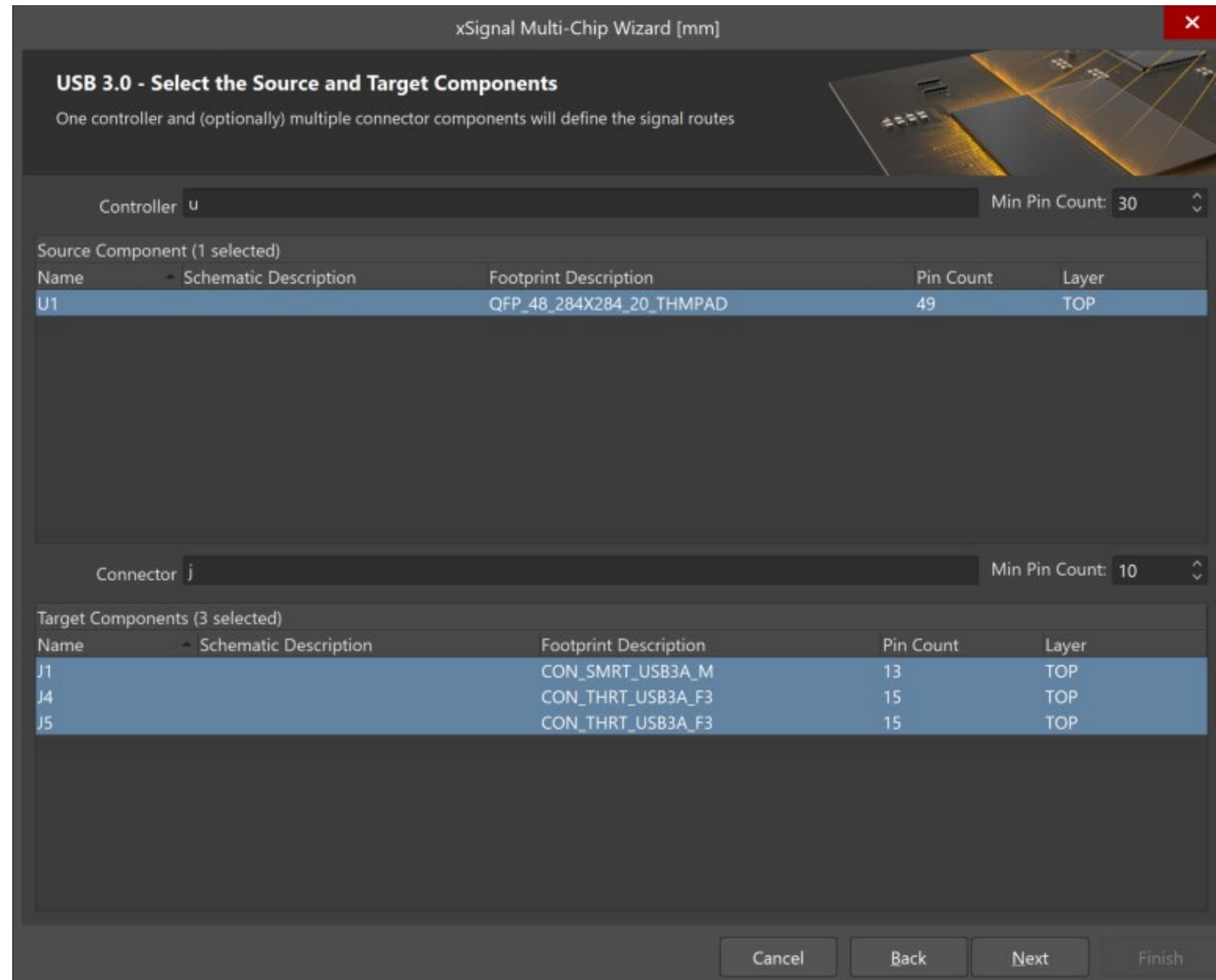


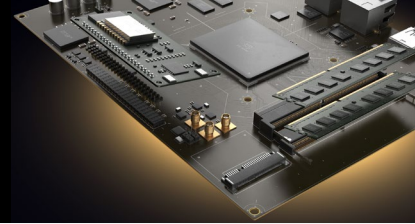


xSignal Wizard:

USB 3.0

- The USB Wizard will add length matching for the diff pairs.
- Allows selection of multiple connectors
- TI USB 3 reference:
<http://www.ti.com/lit/an/spraar7g/spraar7g.pdf>

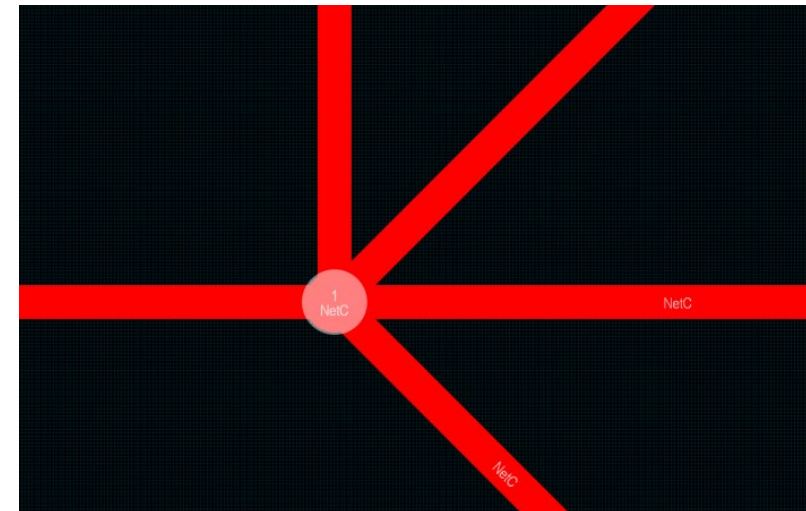
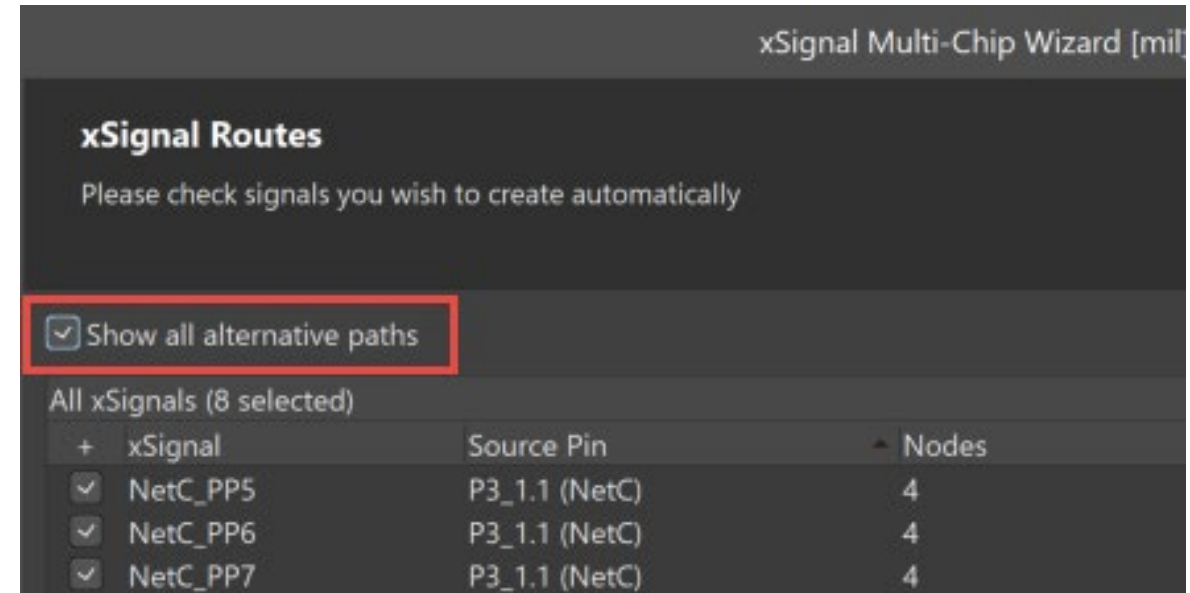




xSignal Wizard:

Custom Multi-Component Interconnect

- Looks at all signals between source and target components.
- Allows to select specific nets or use a net class to constrain nets to include.
- Generates Length Matching rules for the generated xSignals.
- For signals that branch, enable the Alternate Path checkbox to see all routes between the source and targets.





USB 3.0

The MiniPC has a multiplexed USB.

Run xSignal wizard

Custom multi-Component Interconnect.

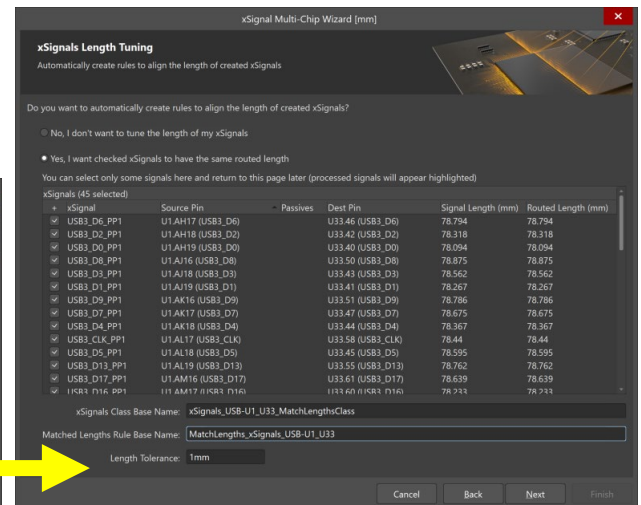
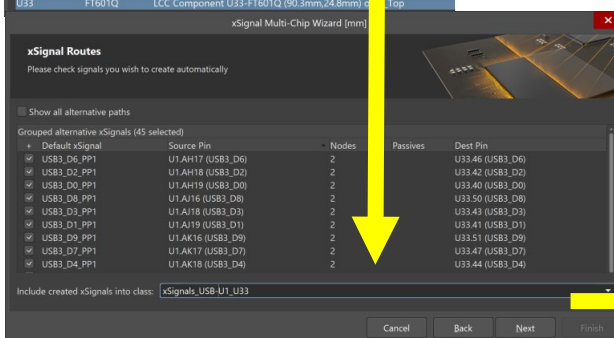
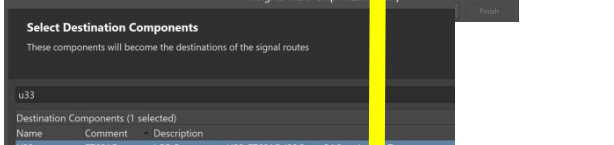
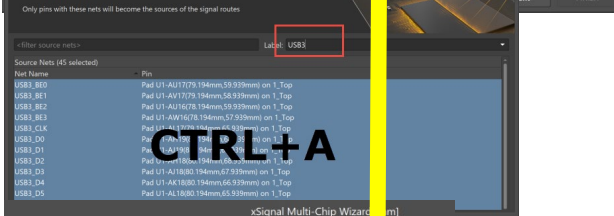
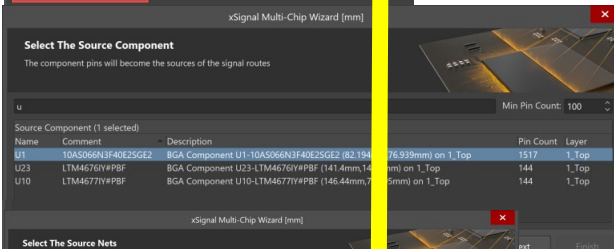
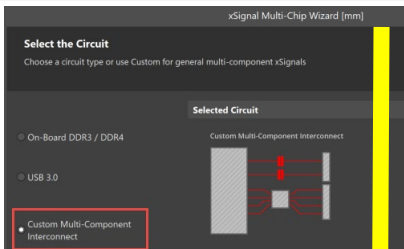
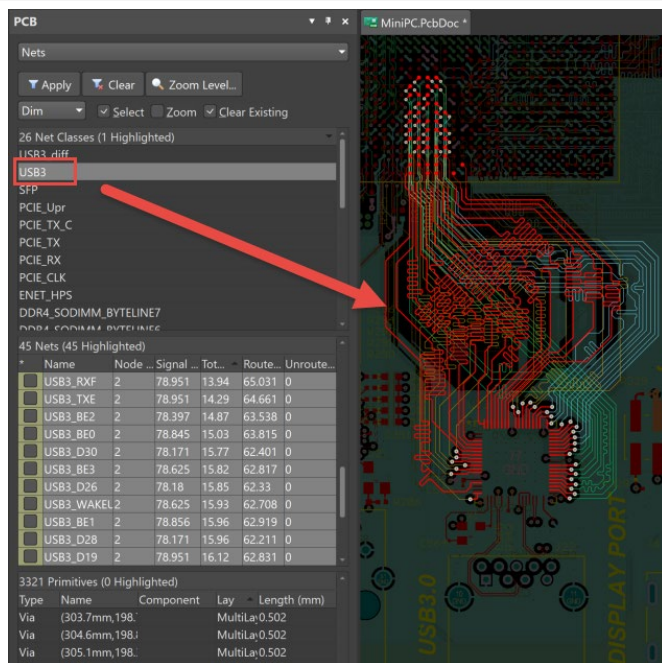
Source: U1

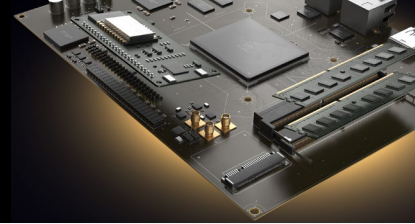
Select USB3 Net Class

Target U33

1mm tolerance

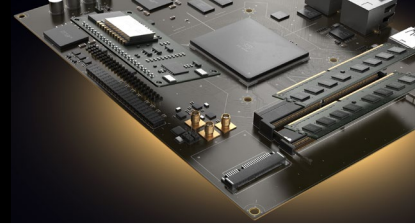
(Add USB in generated names to help differentiate)





AltiumLive 2018

DEMO



AltiumLive 2018 Questions?